International Journal of Research and Development in Engineering Science
ISSN: 2582 - 4201(Online) , http://www.ijrdes.com/
Regular Issue, Vol. 7, Issue. 5 (September – October) , 2025 , Pages: 37 – 41
Received: 24 March 2025 ; *Accepted*: 02 October 2025 ; *Published*: 21 October 2025
https://doi.org/10.63328/IJRDES-V7RI5P8
Original Paper : Laboratory Research – Experimental Research Paper

Smart Thermal Control for Next-Gen 3D ICs

M. Siva Kumar [1*], **J. Mohanraj** [2]

[1-5] Department of Electronics and Communication Engineering, VelTech Rangarajan Dr Sagunthala R&D Institute of Science and Technology, Avadi, Chennai. 600061, India; m.sivakumar450@ gmail.com , jmohanraj@veltech.edu.in

**Corresponding Author: M. Siva Kumar ; m.sivakumar450@ gmail.com*

Abstract: Through TTSV, One of the emerging technologies that is well-suited to CMOS implementations is 3D IC integration, which entails vertically stacking many IC layers. Through Silicon Vias (TSVs) and Cu-Cu bonding are used to physically and electrically connect the IC layers of a 3D IC. Important restrictions in 3D IC designs that have a significant effect on overall system performance are thermal issues between layers and noise coupling between TSV-to-substrate and TSV-to-TSV. Heat spreaders and thermal through silicon vias (TTSVs) play crucial roles in 3-D IC integration. The failure of an integrated circuit (IC) is often caused by excessive heat building up in one area, however heat spreaders and FIN to TTSV have been proposed as solutions in recent years. When a voltage is applied to a three-dimensional integrated circuit (3D IC), the temperature of the IC rises, potentially resulting in the IC's failure. To mitigate this risk, engineers have added fin to the TTSV using a variety of strategies, each of which optimizes the heat dissipation in a different direction. Both carbon Nanotubes (CNTs) and Graphene, which are used for their excellent thermal cooling properties, are widely disseminated. Using ideal orientations and heat spreaders, this study demonstrates a FIN that effectively disperses heat in all directions and transfers thermal energy to a heat sink. We also showed how different thermal cooling effects affect the IC's potential distribution in different circumstances. Based on our findings, Carbon Nanotubes (CNTs) are more effective than Graphene in dissipating heat away from both heat sources and TSVs. We tested the effects of changing the dielectric properties of the model by including Al2o3, Si3N4, and SiO2 as examples.

Keywords: 3D IC, Thermal through silicon Noise Coupling, Heat source, CNT, FIN.

1. Introduction

Since the transistor is the primary building block of electronics, MOSFETs play a crucial role in the IoT. One method for developing compact electronic goods is MOSFET scaling, which is described by Moore's law for contemporary technology. Since the IC is flat, increasing the size of the transistor to save manufacturing space necessitates more metal layers. Wire delays and wire density both increase due to the presence of these metal layers[1-5]. Manufacturing ICs becomes more difficult when parasitic capacitance rises due to the increased wire density. Parasitic capacitance dominates and causes delays in interconnects.

The connection latency became an issue with the transistor delay. As scalability increases, however, the issue of connection latency becomes more pressing [6-7]. Concern about the need to decrease connection latency arose inside the IC. An alternate technique that has shown promise is the three-dimensional integrated circuit. The IC is studied in all three dimensions. Current Conspirator There is a trade-off in terms of system performance when using two-dimensional integrated circuits (2D IC) because of their lower device packing densities[8-10]. The Three-Dimensional Integrated Circuit (3D IC) has replaced the Two-Dimensional Integrated Circuit (2D IC) as the state-of-the-art technology due to its increased signal bandwidth and ability to host millions of devices. In addition, the advent of 3D IC technology and heterogeneous integration has made production for the semiconductor industry more easier. The thermal resistance measures how much heat is lost from the chip's circuit junction to its outside. By cooling the semiconductor, thermal flow limits thermal resistance. The thermal resistance of a chip increases with the number of layers it has. Due to the small size of the devices used in 3D IC, cross-couplings form between the various components in the layer[11-12].

Cross-talk is another name for cross-coupling. When there is less space between the layers, communication between them improves. This is a major problem with the 3D IC design. Additionally, integrated circuits suffer from the issue of vertical cross-talk. An IC may have cross-talk

ISSN: 2582 - 4201(Online) , http://www.ijrdes.com/ , IJRDES, Vol. 7, Issue 5, 2025 , https://doi.org/10.63328/IJRDES-V7RI5P8

between its active layers. Layer stacking on a high-quality semiconductor is damaging to the manufacturing method [13]. Getting rid of or making good use of interference is the first step in fixing 3D IC's main issue. To solve this issue, several different circuits will be constructed. The main restrictions of 3D technology are noise coupling and thermal issues. Noise coupling is the connection between the use of high-performance materials for thermal management in 3D IC design, including silicon nitride (Si3N4), aluminum oxide (Al2O3), and silicon dioxide (SiO2).

2. Related Work

Because of the weak electrical communication between TSVs and Si substrate, which causes noisy coupling disturbances between aggressive and victim TVs and between active devices and Si substrate, this three-dimensional IC integration is primarily motivated by this issue [14-16].

2.1. Model Description using TSV

The problem of noise coupling between TSVs and the Si substrate may be solved by using the right technique. This TSV-based 3D IC suffers from the same noise coupling and heat problems as its 2D counterpart. ETSV, which is nothing more than electrical through silicon-via, experiences noise coupling as a consequence of insufficient electrical signaling, while TTSV, which is nothing more than thermal via silicon-via, experiences heat as a result of increasing heat. Three-dimensional integrated circuits have a higher applied potential[17-18]. With this work, we propose a solution to the stated problem, which is that the effect of heat on an integrated circuit (IC) varies depending on the direction in which the heat travels [19-20]. For instance, if heat is transferred from the heat source to the heat sink in a single direction, the IC may be damaged.

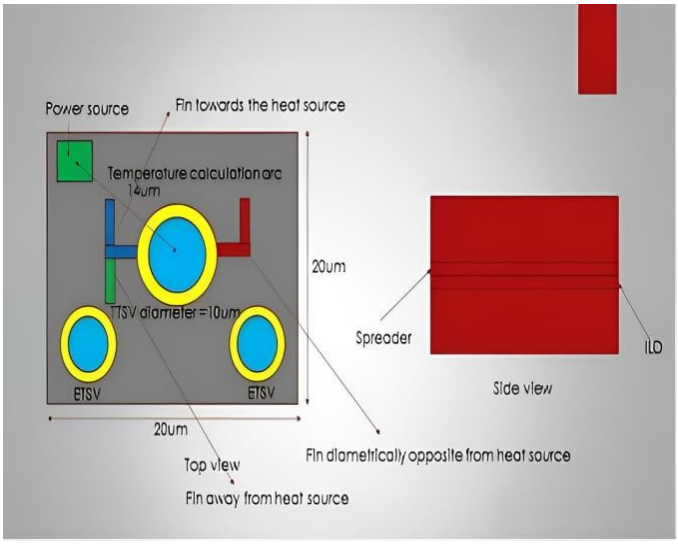

Fig.1 Proposed technique of FIN in various directions

Figure.1 shows the thermal management efficiency of a two-stacked structure, which is analyzed using fins and spreaders with CNT and Graphene as test materials. The impact on signal integrity and heat dissipation from a 1μW hotspot (1μm × 1μm × 0.5μm) is also evaluated. In this article, I'll explain how traditional Three-Dimensional Integrated Circuit (3D IC) architecture and graphene-based FIN heat spreaders work together to provide an optimal heat-management solution. To further address the issue of the IC's TTSV without FIN and with a heat spreader (graphene & CNT), we turn the fin towards the heat source and the fin towards the cylinder. This demonstrates how heat impacts in different directions.

Table.1 Suggested material for Fin and Spreaders for effective thermal management

	CNT	GRAPHENE
Thermal Conductivity	6600(w/mk)	2600(w/mK)
Density	1300kg/m3	1800kg/m3

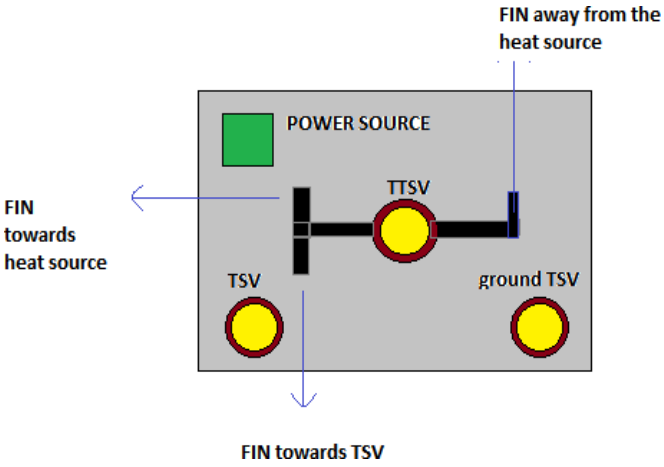

Fig.2.Simulated proposed structure.

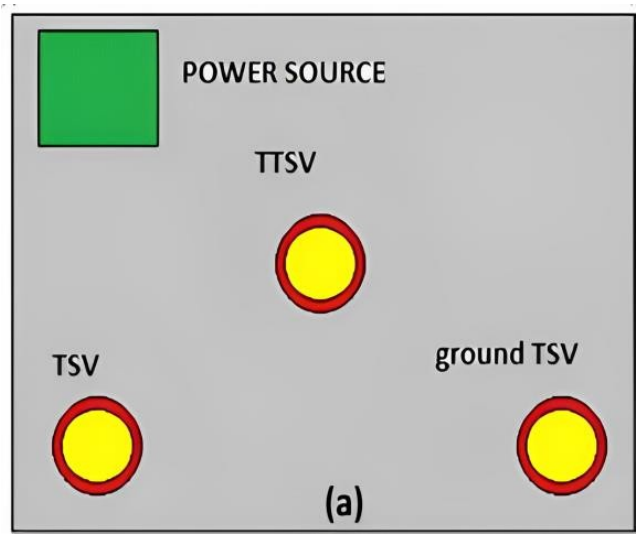

Fig.3 Simulated structure of TTSV without FIN.

ISSN: 2582 - 4201(Online) , http://www.ijrdes.com/ , IJRDES, Vol. 7, Issue 5, 2025 , https://doi.org/10.63328/IJRDES-V7RI5P8

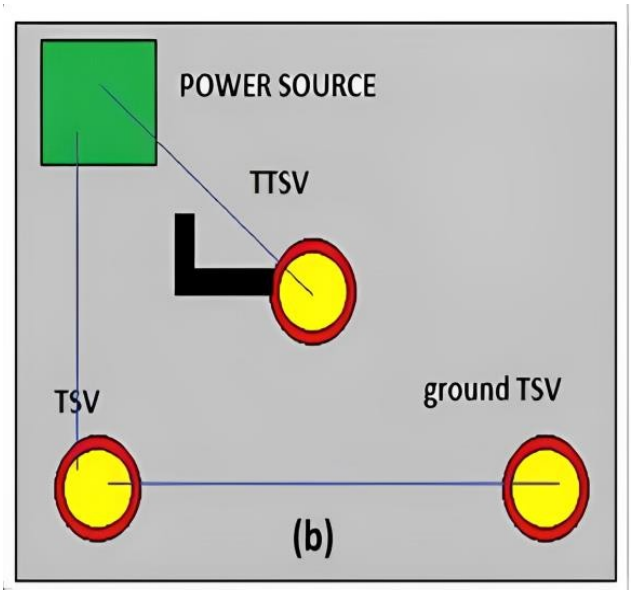

Fig.4.Simulated structure of TTSV with FIN.

Diagram 2 presents a thermal management system incorporating fins and TSVs to facilitate heat dissipation. The fins help in directing the heat towards the TSV, ensuring efficient thermal regulation. Heat is managed by guiding it away from the power source, minimizing localized overheating.

Figure 3 displays the power source along with thermal and ground TSVs, emphasizing their structured placement. The arrangement plays a crucial role in both heat dissipation and electrical connectivity. By strategically positioning the TSVs, thermal pathways are optimized for better performance.

Figure 4 illustrates a power source connected to TSVs and a thermal TSV, integrating an additional element to improve heat dissipation.

This structural component aids in maintaining stable thermal conditions within the system. The overall design ensures an effective balance between heat dissipation and electrical functionality. Proper distribution of heat enhances the reliability and efficiency of the setup.

The combination of TSVs and additional thermal structures supports optimal system performance while preventing thermal bottlenecks.

Table 2. Dimensions of TSV as per ITRS Roadmap

Outer Diameter of TSV	1µm
Outer Diameter of TTSV	1µm
Width and length of Silicon substrate	10µm
Depth of FIN	Variable
Height of silicon substrate	10µm

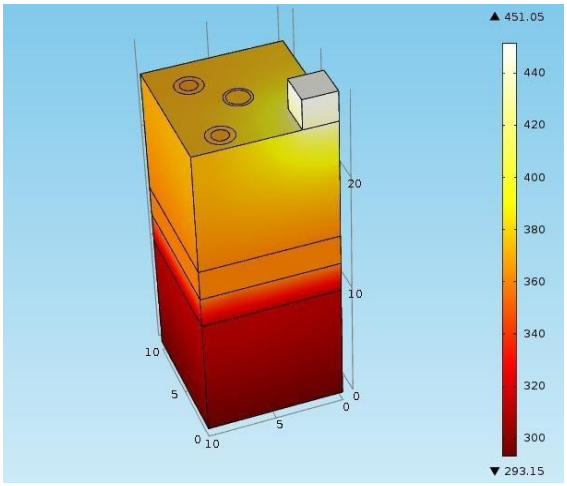

Fig.5.Simulated architecture TTSV without FIN

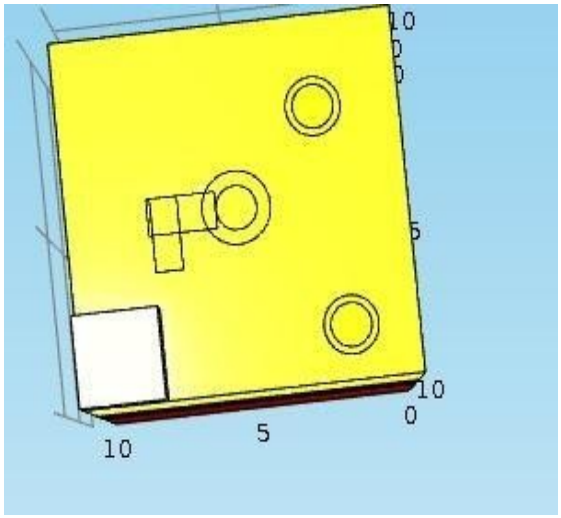

Fig.6 Simulated architecture TTSV with FIN towards heatsource

The heat spreader coating on the fin improves performance when the fin is oriented away from the TTSV and towards the heat source. There was a comparison made between the simulated reference structure with and without TTSV. Clearly shown in Fig 5 is the improved heat transfer performance afforded by a 3D layer structure using TTSV. CNT outperforms Graphene in the thermal management of a three-dimensional IC by using a FIN path with a cylinder, and heat transmitted via a possible source in the direction of the heat source has greater thermal management than heat transmitted via a direction towards the cylinder, which has less thermal management and its simulated architecture shown in Fig.6.

3. Results

Demonstrate the superior thermal cooling effect of CNT-constructed FIN over TSV. CNT's thermal cooling capacity means FIN seldom budges in temperature. TSV generates more total heat than FIN with CNT because of its extreme temperature swings shown in Fig 7. Because it absorbs so much heat, it damages integrated circuits. Since it

ISSN: 2582 - 4201(Online) , http://www.ijrdes.com/ , IJRDES, Vol. 7, Issue 5, 2025 , https://doi.org/10.63328/IJRDES-V7RI5P8

generates less heat, there is less of a danger of IC failure.

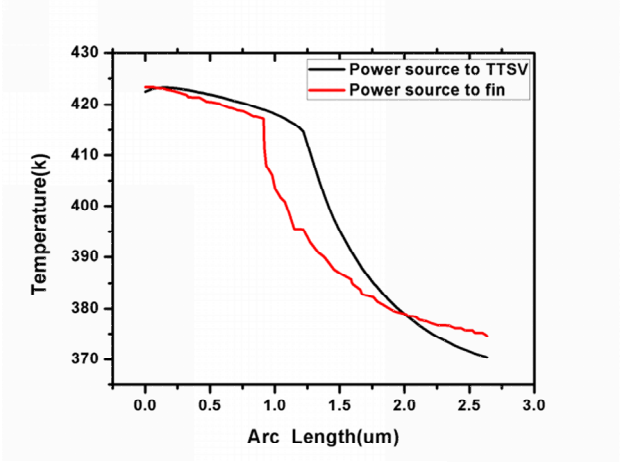

Fig.7.FIN with CNT FIN towards heat source.

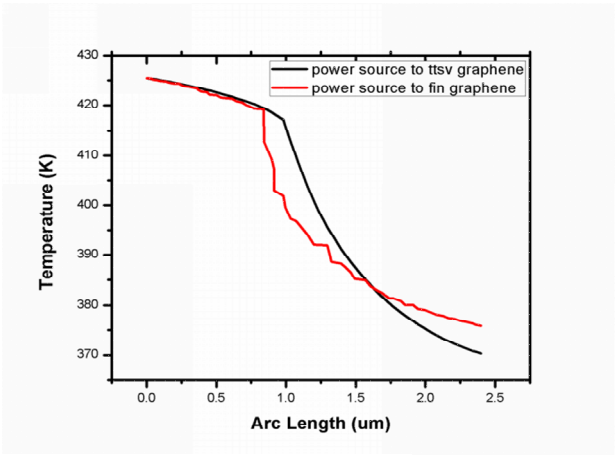

Fig.8 Graphene FIN facing the heat source.

FIN and TSV temperature changes are seen in Fig. 8. The temperature fluctuations are similar to TSV since the FIN is Graphene, which has limited thermal conductivity. The Graphene FIN collects heat from the source, similar to the TSV.

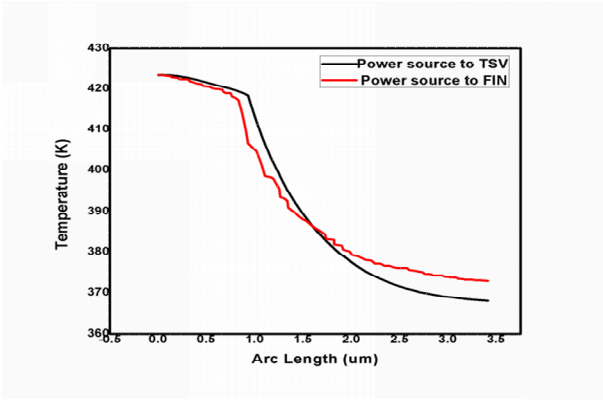

Fig.9 CNT-based FIN with a TSV-leaning orientation.

Figure 9 shows the temperature changes of a CNT-built TSV and FIN power supply. The rapid heat conduction of CNT material makes the power source to FIN cool faster than TSV.

The power source to TSV settles near temperature, and the FIN to power supply FIN is CNT.

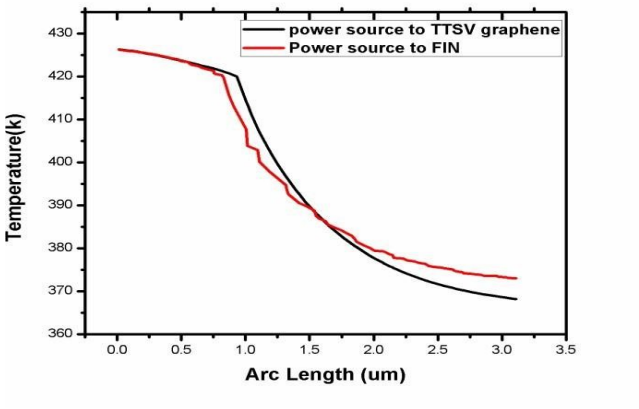

Fig.10. Graphene-based FIN facing TSV.

Fig.10 demonstrates temperature change with Graphene-based FIN and TSV power sources. The accompanying chart shows that power source temperature varies similarly for TSV and FIN. The limited heat conductivity of Graphene causes this.

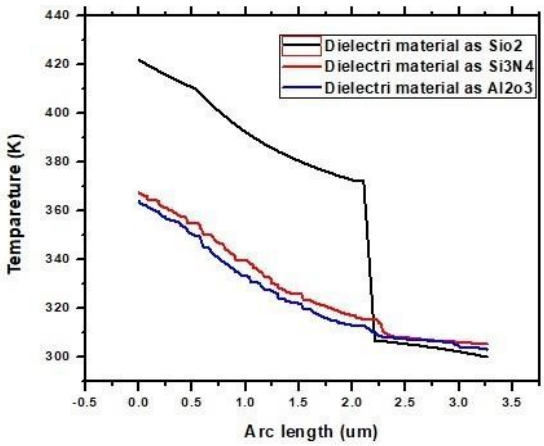

Fig.11 Comparison of Al2o3,Sio2,Si3n4

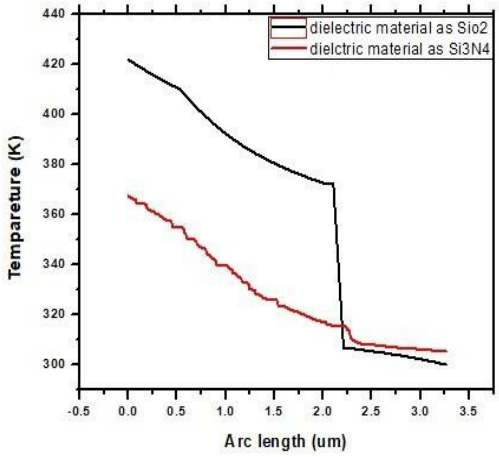

Fig.12 Comparison of Sio2, Si3n4

Figure 11 illustrates the thermal behavior of Through-Silicon Vias (TSVs) under specific conditions. It highlights temperature variations across different regions, showing thermal gradients and potential hotspots. The results help in understanding heat dissipation efficiency in TSV structures. Figure 12 presents a comparative analysis of

ISSN: 2582 - 4201(Online) , http://www.ijrdes.com/ , IJRDES, Vol. 7, Issue 5, 2025 , https://doi.org/10.63328/IJRDES-V7RI5P8

thermal performance in different TSV configurations. It demonstrates how design modifications impact temperature distribution and overall thermal management. The insights assist in optimizing TSV structures for improved thermal reliability.

4. Conclusion

The temperature has a significant impact on how CNT and Graphene interact with FIN. When compared to FIN combined with Graphene, the thermal cooling effect of FIN combined with CNT is superior. FIN made of CNT and directed towards heat source enhances the IC's temperature resistance and provides better results than FIN made of CNT and oriented towards TSV, and in the examination of the three distinct materials al2o3, si3n4, and sio2, FIN constructed of CNT and orientated towards heat source yields better results than FIN made of CNT and oriented towards TSV. Si3n4 has a greater capacity to inhibit heat transfer than either Al2o3 or Sio2.

References

[1]. Suraj Singh, Asisa Kumar Panigrahi, OmKrishna Singh, and ShivGovindSingh. ”Analysis of grapheme and CNT based finned TTSV and spreaders for thermal management in 3D IC.” In 2016 IEEE International 3D Systems Integration Conference (3DIC), pp.1-4. IEEE, 2016.

[2]. R. S. Patti, “Three-dimensional integrated circuits and the future of system-on-chip designs, “Proceedings of the IEEE, vol.94, no.6, pp.1214- 1224, 2006

[3]. C. C. Liu, I.Ganusov, M.Burtscher, and S.Tiwari, “Bridging the processor- memory performance gap with 3D IC technology, “IEEE Design & Test of computers, vol.22, no. 6, pp. 556-564, 2005

[4]. Y.Akasaka“Three-dimensional IC trends, “proceedings of the IEEE, vol.74, no. 12, pp. 1703-1714, 1986

[5]. K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, “3-D ICs: novel chip design for improving deep-submicrometer.