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Enhancing Grid-Connected Photovoltaic Systems Power Quality through the Unified Power Flow Controller Equipped with an Innovative Sliding Mode and PR Control System

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Abstract: This paper objects to improve power quality in grid-connected photovoltaic (PV) system through development of an advanced Unified Power Flow Controller (UPFC) these participates dual control strategies with the multi-level inverter architecture. UPFC, the flexible and multifunctional power electronic device, addresses common current-related power quality issues—including harmonic distortion, current imbalance, and transient disturbances—by effectively managing power flow and compensating to reactive currents at a point of common coupling (PCC). Here, proposed control scheme employs sliding mode control (SMC) under steady-state conditions and switches to proportional resonance (PR) control during dynamic disturbances, enabling precise and responsive current regulation. In contrast to high-frequency inverters has the switching losses in high-power applications, an inclusion of MLI connected to UPFC design significantly reduces Total Harmonic Distortion and improves inclusive system efficiency. Here, system's efficiency is authenticated through simulations in a MATLAB/Simulink environment, since various working scenarios such as harmonic injection, unbalanced current conditions and transient events, and current swell. Simulation results establish the proposed UPFC configuration noticeably increases current and PCC, PV system's output, and across grid interface. These findings highlight Voltage of UPFC, integrated with MLI, as robust and efficient solution to enhancing current regulation and overall quality power in PV grid-tied systems.
Keywords: Grid Computing , Power Quality, PR Control System, PFCE, Smart Grid, uPFC, PCC, MATLAB.

1. Introduction

The development and implementation of photovoltaic (PV) systems across residential and industrial sectors have been pushed by increasing worldwide focus on renewable energy. In addition to helping achieve environmental goals, switching to green energy will meet growing need to safe and clean electricity. When compared to other renewable energy sources, solar PV stands out to a number of reasons, including its scalability, affordability, and simplicity of installation. However, pledging consistent power high-quality supply was ascended as prime obstacle to PV systems' widespread integration into Electrical grids.

The oscillation and sporadic of solar irradiance, which was direct impact on output current of grid-connected PV systems, is has a giant cause to concern in this paper. Harmonics, imbalances in current and reactive power are only the few power quality problems these may result from these oscillations. In addition, a power electronic converters used in PV systems are not linear by design, which means they supply extra harmonic currents to a grid. These problems, if left unchecked, may reduce a efficiency of delicate machinery, lead to overheating, heighten power losses, and reduce a life of electrical parts. Consequently, urbane reimbursing devices and management measures are mandatory to quality power in such uncertain and ever-changing environments.

Historically, high-voltage transmission systems have made use of UPFC, a central component of the family from FACTS, to regulate voltage, phase angle, and impedance. Renewable energy systems and distribution networks have begun to use it more extensively in recent years. An ultra-powerful rectifier (UPFC) was great device to quality power improving in PV array systems these are linked to grid because of its unique capacity to control reactive and actual power separately. An upstream power factor correction (UPFC) may reduce harmonic distortion, even out current imbalance, and keep reactive power exchange steady at the point of common coupling (PCC) when it's integrated correctly.

A strong and smart control technique is necessary to completely reap a advantages of UPFC in these kinds of applications. the common challenge to traditional proportional-integral (PI) controllers in PV-integrated grids is a presence of nonlinearities and a quick occurrence of disturbances. On other hand, SMC and other cultured control approaches provide far better resistance to changes in parameters and outside disturbances.

This research presents the new approach to controlling UPFCs these combine a best features of SMC and PR controllers in order to regulate their functioning in conjunction with grid-connected photovoltaic systems. As the power interface between the UPFC and a grid, a multi-level inverter further improves performance. By reducing Total Harmonic Distortion (THD) in an injected current, this inverter design enhances waveform quality and drastically decreases switching losses. To tackle a urgent power quality issues in contemporary PV-integrated electrical networks, the suggested approach integrates intelligent control with efficient hardware design.

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2. Multi-Level Inverter of UPFC and PR

2.1. PR Controller

A PR controller is operated to increase act of VSC under unbalanced operating conditions. The PR controller is particularly actual due to its capability to simultaneously regulate both AC and DC components. It ensures zero steady-state error in DC signal tracking while also providing effective compensation to harmonic disturbances.

As illustrated in the control scheme shown in Fig. 3, there are 2 types of compensation mechanisms are unified. Here, both series & parallel configurations of SMC and PR controllers are inspected to achieve ripple-free voltage of DC-link. Interaction between the two controllers gives critical role in enhancing system stability and dynamic performance. To achieve optimal control design, parameters of PR controller must be sensibly tuned.

The PR compensator is primarily responsible to tracking an oscillatory components, thereby contributing to harmonic mitigation and dynamic response improvement. the commonly adopted form of the PR controller is expressed by the transfer function, in Eq. (5):

$$G_{PR}(S) = K_P + K_R \frac{S}{S^2 + {W_{ACf}}^2}$$

where WACf represents an aC reference(fundamental) angular frequency; KP and KR are a proportional and resonance coefficients of PR controller, respectively. an issue with a PR sort of controller is its incapacity to mitigate for a DC disturbance presented in a control loop by non-linear loads. To prevent this issue, a PR controller is included according to Eq... (6), with KRbetween 0 and 1 and WACf 2 = 1.

$$G_{PIR}(S) = K_P + K_I \frac{1}{S} + K_R \frac{S}{S^2 + W_{ACf}^2}$$

where KI is an integral coefficients. Figure. 4 shows "Figure X presents a block diagrams of a practical and ideal PR controllers. an ideal PR controller is characterized by a following transfer function:

$$G_{PRh}(S) = K_{Ph} + K_{Ih} \frac{S}{S^2 + h^2 W_{ACf}^2}$$

In this expression, *h* indicates a harmonic order. a transfer role of a practical PR controller can be written as:

$$G_{PRTh}(S) = K_{Ph} + K_{Ih} \frac{(W_C S + hW_C^2)}{S^2 + 2W_C S + \left(W_C^2 + h^2 W_{ACf}^2\right)}$$
$$\approx K_P + K_I \frac{W_C S}{S^2 + 2W_C\ S + h^2 W_{ACf}^2}$$

The cutoff frequency of a PR controller, denoted as act, plays the crucial role in regulating current errors at a fundamental (zero-harmonic) frequency under steady-state conditions. a PR controller achieves this regulation through a combined action of a proportional gain KI and a resonant term RI(s). a resonant term is modelled as the second-order filter with zero damping and the resonant frequency of h·ωACf by increasing ωACf in the practical PR design, a system bandwidth expands, improving its ability to tolerate grid frequency variations.

Alongside a PR controller, the Sliding Mode Control (SMC) scheme is also applied. In SMC, a system initially undergoes the reaching phase in which its trajectory is driven toward the predefined sliding surface in a state space. When this surface is reached, a system enters a sliding mode, where its motion is constrained to a surface, providing robustness against disturbances. a SMC design requires selecting the suitable sliding surface—defining a desired dynamic behaviour—and constructing the control law these forces and maintains a trajectory on these surface. a sliding surface employed in this work, defined in Eq. (9) and denoted Ss(t), forms a basis to achieving a required robustness.

$$S_s(t) = K_p er + K_i \frac{d}{dt}\ er$$

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The control law is formulated using error time, denoted as ere_rer, which signifies change between reference and actual voltage, either direct d-q-axis of system. This error serves as driving force to guide system toward desired state. To fine-tune reply and achieve best performance, control law integrates two adjustable parameters: proportional gain Kp and integral gain Ki. By applying this control law, system is compelled to converge to steady-state condition where error is minimized, ensuring these system closely follows reference signal and maintains reliable operation under varying conditions:

$$S_s(t) * \dot{S}_s(t) < 0$$

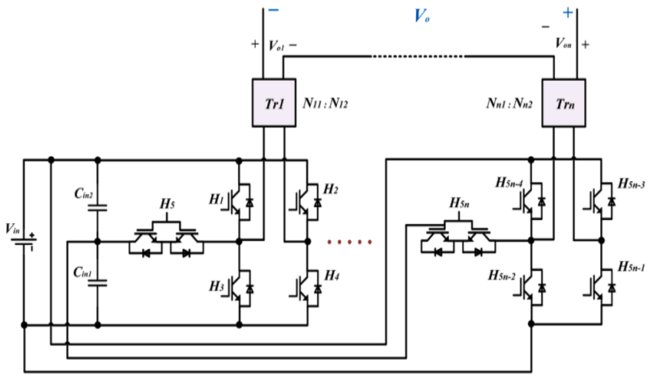

Figure. 1 Layout of a multi-inverter circuit on paper

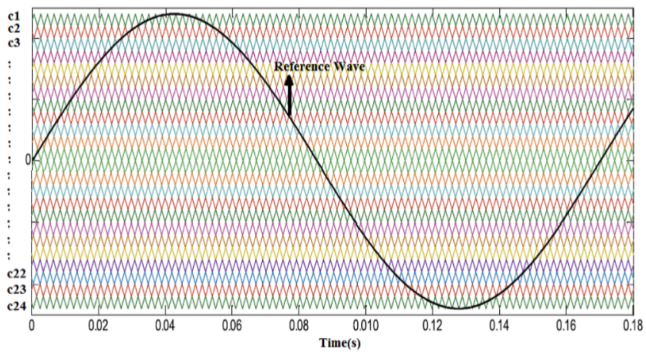

Figure.2 The 25-level inverter's carrier waveforms for the modulation unit's approach using a sinusoidal reference.

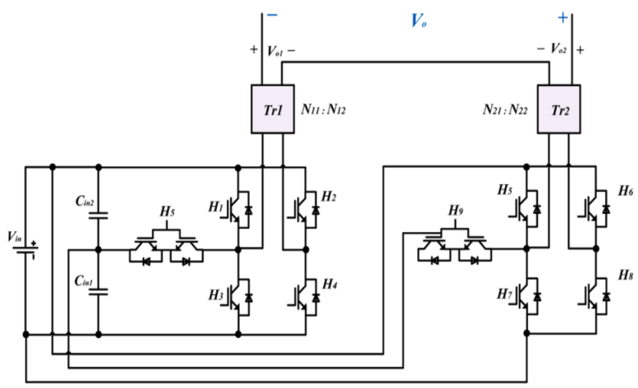

Figure.3 Two sub-inverter units compose the converter. See Table 1 for the single-phase 25-level inverter's look-up.

$$\text{if } S_s(t) > 0 \text{ and } \dot{S}_s(t) < 0, \text{ then } S_s(t) \text{ decreases towards zero}$$
$$\text{if } S_s(t) \langle 0 \text{ and } \dot{S}_s(t) \rangle 0, \text{ then } S_s(t) \text{ increases towards zero}$$

This observation indicates that once a system trajectory aligns exactly with a sliding surface, a reaching mode is effectively terminated.

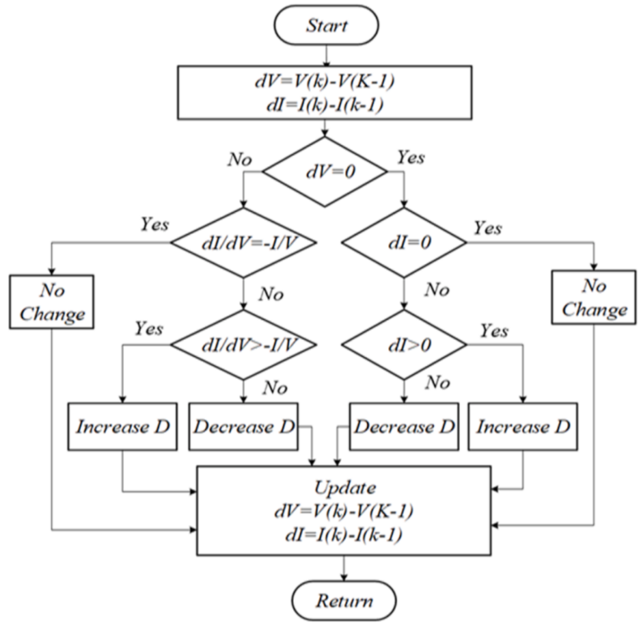

Figure. 4 Flowchart of an iC algorithm.

As the result, both a switching function—often referred to as a change line and its rate of change, or phase swiftness, reduce to zero.

Table. 1 Analysis of Photovoltaic systems parameters marks a transition into a sliding mode

On Switches	V_O(V)	On Switches	V_O(V)
H_5, H_4, H_6, H_7	V_1	H_5, H_2, H_8, H_9	$- V_1$
H_1, H_4, H_6, H_7	$2V_1$	H_2, H_3, H_8, H_9	$-2V_1$
H_2, H_3, H_{10}, H_9	$-2V_1+V_2$	H_1, H_4, H_{10}, H_7	$2V_1-V_2$
H_5, H_2, H_{10}, H_9	$-V_1+V_2$	H_5, H_4, H_{10}, H_7	V_1-V_2
H_1, H_2, H_{10}, H_9	V_2	H_3, H_4, H_{10}, H_7	$-V_2$
H_5, H_4, H_{10}, H_9	V_1+V_2	H_5, H_2, H_{10}, H_7	$-V_1-V_2$
H_1, H_4, H_{10}, H_9	$2V_1+V_2$	H_2, H_3, H_{10}, H_7	$-2V_1-V_2$
H_2, H_3, H_6, H_9	$-2V_1+2V_2$	H_1, H_4, H_7, H_8	$2V_1-2V_2$
H_5, H_2, H_6, H_9	$-V_1+2V_2$	H_5, H_4, H_7, H_8	V_1-2V_2
H_1, H_2, H_6, H_9	$2V_2$	H_3, H_4, H_7, H_8	$-2V_2$
H_5, H_4, H_6, H_9	V_1+2V_2	H_5, H_2,H_7, H_8	$-V_1-2V_2$
H_1, H_4, H_6, H_9	$2V_1+2V_2$	H_2, H_3, H_7, H_8	$-2V_1-2V_2$
H_1, H_2, H_6, H_7	0	H_3, H_4, H_8, H_9	0

This observation indicates these once the system trajectory aligns exactly with the sliding surface, the reaching mode is effectively terminated. As a result, both the switching function—often referred to as the change line—and its rate of change, or phase swiftness, reduce to zero. This marks the transition into the sliding mode, where the system dynamics are confined to the sliding surface, ensuring stable and consistent performance [24].

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$$S_s(t) = K_p er + K_i \frac{d}{dt} er = 0$$

To achieve voltage regulation, an unified Power Flow Controller (UPFC) uses controlled switching devices to generate a compensation voltage (Vc) these is injected in series with the source voltage (Vs) to each phase.

This series voltage injection is implemented using specialized transformers these ensure electrical isolation between an inverter's voltage source and the power grid. an impedance of the grid, or the voltage source, is denoted by Zs. an operational behaviour of an UPFC is defined by a set of mathematical equations these describe an interaction between an injected voltage, source voltage, and the resulting current and voltage waveforms in the system:

$$Ki_{ic} = \left(\frac{u_p V_{dc} - V_c}{L} \right)$$

$$Kv_c = \left(\frac{i_{ic} - i_{sc}}{C} \right)$$

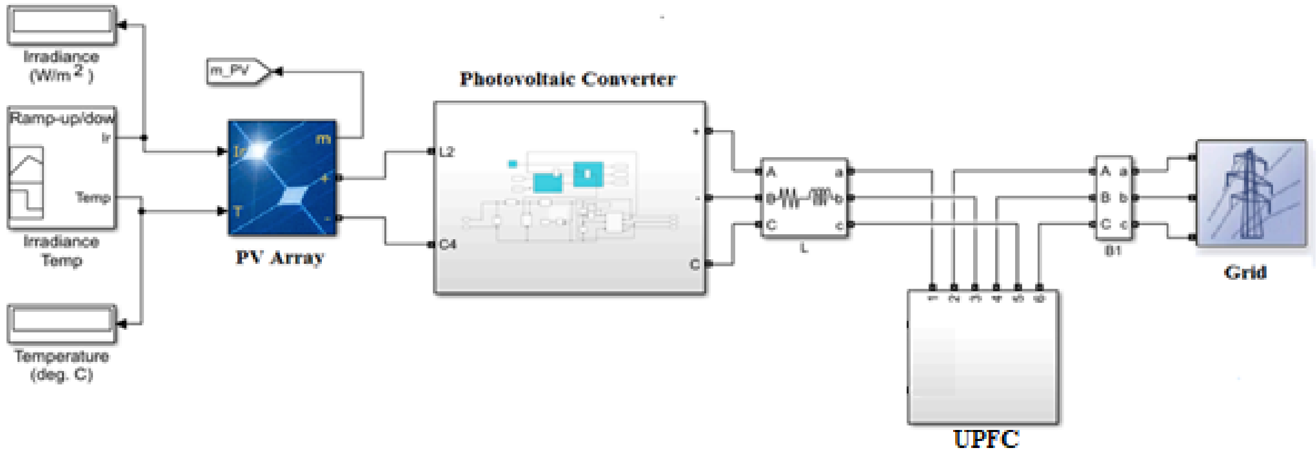

Figure.5 A simulation of a studied system in MATLAB/Simulink software.

Table. 2 Photovoltaic systems parameters

photovoltaic systems parameter	Value
Parallel strings (S_p)	66
Series-connected modules per string (S_s)	5
Module	sun power SPR-305E-WHT-D
Maximum power	305.226 W
Cells per module	96 NCELL
Open circuit voltage (V_{oc})	64.2 V
short circuit Current (I_{sc})	5.96 A
voltage of MPPT (V_{mppt})	54.7 V
Current of MPPT (I_{mppt})	5.58 A
Temperature factor of V_{oc}	−0.2727
Temperature factor of I_{sc}	0.061745
Light-generated current I_L	5.9657 A
Diode saturation Current (I_{DS})	6.3076e-12 A
Diode ideality factor	0.94489
parallel R (R_p)	393.2054 ohm
Series R (R_s)	0.37428 ohm
Photovoltaic capacitor ($C_{photovoltaic}$)	1000 μf

The derivative operator isci_{sc} in a framework specified by given parameters, where K=ddtK = \frac{d}{dt}K=dtd. iici_{ic} is the supply current, and isc is its symbol. Vdc, where iic is the inductor current,

The derivative operator is in the framework specified by given parameters, where K=dot. IIIc is a supply current, and is its symbol. Vdc, where IIIc is a inductor current, a Sliding Mode Controller (SMC) design process consists of two main steps: determining an appropriate sliding surface function and choosing an effective control strategy.

Table.3 UPFC Parameters

DVR parameter	Value
Grid voltage	380 V
Filter inductor L_f	10 mH
Filter capacitor L_f	20 μf
DC supply voltage	350 V
Frequency	50 Hz

It uses the chargeable DC power supply (Vdc), the compensation voltage (Vic), the filter capacitance (C), the filter inductance (L), and the control input (up). Main Aim is to control voltage output of an inverter, which is a same as an injected voltage in the DVR setting.

Both a compensating voltage error and its rate of change may be effectively and simply used as state variables inside an SMC framework. While another method these takes into account both a inverter current error and a compensating voltage error might potentially achieve good results, it would make controllers more complicated and expensive since more current sensing would be required. Therefore, in order to include it into the control design, it is advised to establish the compensation voltage error and its derivative:

$$X_1 = V_c - V^*_c,\ X_2 = \dot{X}_1 = \dot{V}_c - \dot{V}^*_c$$

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In this context, $\dot{X}1$ represents the derivative of X1, and Vic is the derivative of the compensating voltage Vic, where Vic itself serves as the reference to the compensation voltage generation. Equation (14) clearly indicates these an accurate value of Vic is essential to the proper operation of the voltage regulation scheme. By taking the derivatives of both X2 and X1, the resulting expressions provide the dynamic behaviour of the system, which is necessary to constructing the sliding surface and designing the control law. These derivatives play a key role in shaping the control response and ensuring the system accurately tracks the desired compensation voltage under varying grid conditions.

$$X_1 = V_c - V*_c, X_2 = \dot{X}_1 = \dot{V}_c - \dot{V}*_c$$

Substituting (9) into $\dot{X}2$ yields

$$\dot{X}_2 = \frac{-K\dot{V}^*{}_c + (Ki_c - Ki_s)}{C}$$

Using $V_c = X_1 + V^*{}_c$ and $W_s{}^2 = \frac{1}{LC}$

In resultant equation, after substituting equation (12) into equation (16), we obtain unified expression these describes system's dynamic behaviour in terms of compensating voltage error and its derivative. This substitution integrates defined state variables and control input, enabling more compact and tractable form to sliding mode control design. resulting expression effectively captures relationship between compensation voltage, its reference, and control effort required to drive error to zero, forming foundation to ensuring robust voltage regulation within system:

$$\dot{X}_2 = \frac{-W_s{}^2 X_1 + W_s{}^2 u_p V_{dc} - W_s{}^2 V^*{}_c - K\dot{V}^*{}_c - (Ki_s)}{C}$$

Therefore, DVR's movements in relation to state variables X1 and X2 can be expressed through set of differential equations these represent system's dynamic response. Precisely, X1, distinct as voltage error (Vic∗−Vic), and X2, derivative of X1, together describe how DVR reacts to voltage disturbances. These state variables allow controller to monitor both magnitude and rate of change of voltage deviation. By manipulating control input up, DVR adjusts its injected voltage in such way these X1 and X2 converge to zero, thereby restoring voltage at PCC to its reference value and maintaining power quality.

$$\dot{X}_1 = X_2$$

$$\dot{X}_2 = W^2{}_s \left[u_p V_{dc} - X_1 + D(t) V_{dc} \right]$$

When a disturbance denoted by D(t) is:

$$D(t) = \frac{-LKi_s - V^*{}_c - LCK\dot{V}^*{}_c}{V_{dc}}$$

The function D(t) exhibitions clear time requirement, demonstrating these system's undercurrents are unfair by varying time frames. This behaviour is given in Eq. (20), which accentuates need to robust control strategy to handle such variations effectively. Sliding surface function, which is central to design of SMC, is characterized to guide system states toward desired equilibrium point. It is typically defined linear combination of error and its derivative:

$$S = \lambda X_1 + X_2$$

Here, λ denotes positive descending parameter these directs rate at which system converges to sliding surface. system enters sliding mode when sliding condition is satisfied, meaning both sliding function SSS and its derivative $\dot{S}$ are equal to zero, i.e., $S = \dot{S} = 0$. This condition ensures these the system's state trajectory is confined to the sliding surface and directed towards an equilibrium point at an origin, where X1=0 and X2=0.

The dynamics of the system in the sliding mode can be expressed by the following equation:

$$\dot{X}_1 = X_2 = -\lambda X_1$$

Deriving the solution to Eq. is relatively simple. (22) as:

$$X_1 = X_1(0) e^{-\lambda t}$$

To ensure these an error variables remain on the sliding surface and ultimately converge to an origin, the following conditions—known as reachability or sliding mode existence conditions—must be satisfied:

$$S\dot{S} < 0$$

Presence of sliding system stability and robustness under parameter uncertainties and external disturbances. To ensure the system enters and remains on the sliding surface, the control input up must be defined in a way these satisfies the sliding condition and drives an error dynamics toward an origin.

The control input up is typically formulated as:

$$u_p = -sign(S)$$

If the following conditions are fulfilled, the sliding mode will persist in operation, ensuring these the system remains on the sliding surface and exhibits the desired dynamic behaviour:

Situation 1: When S < 0 ⇒up = 1

$$\dot{S} = -W^2{}_s X_1 + \lambda X_2 + d_1(t) > 0$$

Situation 2: When S > 0 ⇒up = − 1

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$$\dot{S} = -W^2{}_s X_1 + \lambda X_2 + d_2(t) < 0$$

In Ess. (26) and (27), the functions d1(t) and d2(t) represent the time-varying boundaries these define the region within which the sliding mode exists on the (X1,X2) phase plane. These boundaries form two simultaneous lines, and the region enclosed between them corresponds to the permissible domain where the system's trajectory can sustain sliding motion.

Mathematically, d1(t) and d2(t) are described as:

$$d_1(t) = W^2{}_s V_{dc} + D(t)$$
$$d_2(t) = -W^2{}_s V_{dc} + D(t)$$

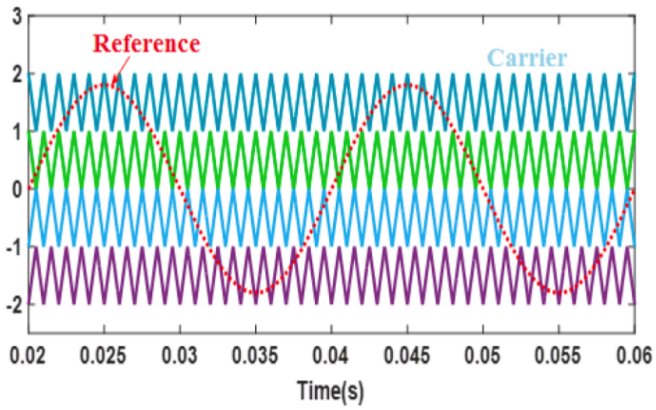

Figure. 6 Waveforms of modulation

The critical factor determining a rate of convergence of the compensation voltage error in sliding mode control (SMC) is a parameter λ, as shown in Eq. (23). While a bounds of an existence area inside the phase plane are not clearly shown in Ess. (26) and (27) because of spatial restrictions, it is clear these λ does determine them. a stability and robustness of the sliding mode may be compromised due to a narrowing of a existence area caused by the greater value of λ, which leads to quicker dynamic reaction.

On a other hand, the DVR or UPFC, which are fast-acting compensators, may not enjoy a slower reaction caused by the lower λ value, even if it widens a existence area.

To achieve the fair trade-off between stability and reaction speed, it is crucial to find an acceptable λ. Although heuristic techniques have historically been used to tuning λ, analytical methods have been suggested in more recent research to find an ideal value.

Maximizing an existence region while improving a dynamic performance of the compensation mechanism is a goal of these strategies. The system's frequency response and damping characteristics are affected by a properties of an output LC filter, which in turn impact an appropriate.

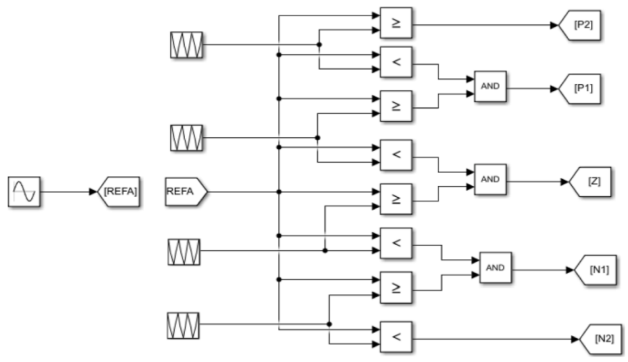

Figure.7 Modulation unit

λ value. a technique outlined in reference [33] is followed in this work to determine λ, guaranteeing the balance in control system performance these is both theoretically sound and practically effective.

3. Multi-Level Inverter of UPFC

An improved Cascaded Transformer Inverter (ICTI) is the multilayer inverter design these is schematically shown in Figure 1. voltage divider with 2-level capacitor, VDC, and several SIUs with transformers make up this novel setup. To be more precise, the system requires five SIUs, each of which is connected to separate DC source and parallel capacitors, of two usually charged to half the DC voltage. a bidirectional switch and H-bridge cell integrated into each SIU allow to a development of five independent voltage levels. For galvanic isolation and voltage transformation, an Citi arrangement relies on single-phase low-frequency transformers. This makes sure these a separate DC sources can still provide power to each inverter unit. When connecting an inverter source to the secondary transformer side, it is essential to use the cascaded transformer design to provide proper electrical isolation. More step-up transformers may be added to the system in order to get a high-voltage output from a low-voltage input.

The use of asymmetric multilevel inverter principles in an Citi is particularly noteworthy since it enables a development of greater output voltages with fewer semiconductor switches. a turn ratios of the transformer determine the number of usable voltage levels, and there are the variety of ways to find these ratios. There are many combinations of switching states across Citi modules these cause an inverter to produce varied output voltages. the broad variety of voltage levels may be created by managing the voltage imbalance among a outputs of transformers. In an end, a output phase voltage of an inverter system is improved by adding together a different transformer outputs.

$$V_{output} = V_{output\ 1} + V_{output\ 2} + \ldots + V_{output\ n}$$

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In this context, the variable *n* denotes the number of Sub-Inverter Units (SIUs), which correspond to the cascaded transformer stages in the multilevel inverter configuration. By appropriately selecting the turn ratios of these cascaded transformers, an output voltage of an inverter can be effectively regulated to meet the desired level. If all the transformer turns ratios in the configuration, as showed in Figure. 5, with equal and represented with ϱ, an inverter operates as symmetric multilevel inverter**.** Under this symmetric condition, the no. of distinct voltage output levels (*ml*) these an inverter can generate is directly related to the number of SIUs (*n*), and this relationship can be mathematically expressed as:

$$ml = 4n + 1$$

This equation indicates these a symmetric configuration with *n* SIUs can produce an output with *(2n + 1)* distinct voltage levels, enhancing the resolution and quality of the synthesized waveform.

An *n*-cascaded Improved Cascaded Transformer Inverter (ICTI) configuration, assuming a **symmetric design** where all sub-inverter units (SIUs) have the same transformer turn ratio ϱ and each is powered by the same DC voltage source Vdc

$$V_{out\ max} = n.\rho.V_{dc}$$

In asymmetric Improved Cascaded Transformer Inverter (ICTI) configurations, where transformer turn ratios differ across sub-inverter units (SIUs), a broader and more flexible range without increasing the number of semiconductor components output voltage levels can generated . This flexibility arises from the strategic selection of transformer turn ratios based on **a** geometric progression**.**

In this study, the turn ratios are chosen using geometric progression with common ratios such as **2**, **3**, and **5**, with the progression based on 5 referred to as the **"finery" strategy**. By applying such geometric progressions, the voltage steps contributed by each SIU differ in magnitude, enabling an inverter to synthesize a more diverse and granular set of output voltage levels.

Output voltage are represented as blends of:

$$ml = 2^{n+2} - 3 \ \frac{N_{i2}}{N_{i1}} = 2^{i-1}\rho \ i = 1, 2, \ldots, n$$

$$ml = 2\left(3^{n} - \frac{1}{2}\right) \frac{N_{i2}}{N_{i1}} = 3^{i-1}\rho \ i = 1, 2, \ldots, n$$

$$ml = 5^{n} \ \frac{N_{i2}}{N_{i1}} = 3^{i-1}\rho \ i = 1, 2, \ldots, n$$

$\frac{N_{12}}{N_{11}}$ or in a symmetric configuration, each transformer has the same turn ratio ϱ:

The maximum output voltage in this case is the sum of the voltages contributed by each SIU in the positive switching state:

$$V_{out\ max} = V_{dc}\sum_{i=1}^{n}\frac{N_{i2}}{N_{i1}} = V_{dc}\cdot\rho\sum_{i=1}^{n}\mathscr{T}^{i-1}$$

This formula gives the maximum unipolar voltage level attainable using an asymmetric ICTI configuration with a geometric progression of transformer turn ratios.

Another critical consideration in design of multilevel inverters is voltage rating of semiconductor switches. These ratings significantly impact both cost and practical realization of an inverter. The higher progression factor allows to broader range of output voltage levels, contributing to improved waveform quality and lower harmonic distortion.

In an CTI architecture, each inverter unit incorporates two types of switches: unidirectional and bidirectional. These switches experience different voltage stresses, which determine their required blocking voltage capability.

$$VS_{UNI} = V_{dc}$$

$$VS_{BI} = \frac{1}{2}V_{dc}$$

Various strategies have been developed to symmetrical MLC, typically adapted from conventional techniques used in traditional converter designs. Among these, the most widely adopted method is PWM is extensively utilized in multilevel inverters (MLIs) to control an output voltage and improve an efficiency of power conversion. In MLIs, PWM functions by producing a series of voltage pulses whose widths are modulated to approximate a sinusoidal waveform.

The core concept of multi-carrier PWM involves comparing a sinusoidal reference signal with multiple carrier signals these are vertically shifted. To achieve ml output voltage levels**,** ml − 1 carrier signals are required. As illustrated in Figure. 6, the modulation scheme to a 25-level inverter uses 24 carriers (a1,a2,...,a24), each positioned with incessant bands around zero-reference level. These carriers share amplitude Ac and freq fc, while the sinusoidal reference wave has an amplitude AR and frequency for. At every moment, an outcome of the comparison between the reference and the carrier signals determines an appropriate switching function to generate the corresponding output voltage level.

Figure.7 presents the model of the proposed converter, which includes two sub-inverter units used to define the switching table. the sub-inverter can produce output voltages of 0,V1,2V1and −2V1 , while 2 sub-inverter is capable of generating 0,V2,2V2,−V20, V_2, 2V_2, -V_20,V2 ,2V2,−V2, and −2V2-2V_2−2V2. This implies these the transformer turns ratios associated with these sub-inverters are specifically chosen to support this range of output levels.

$$\frac{N_{11}}{N_{12}} = \frac{V_{in}}{2V_1}$$
$$\frac{N_{21}}{N_{22}} = \frac{V_{in}}{2V_2}$$

Assuming these each phase contains two inverter units, the corresponding switching table is established as shown in Table 1. This table outlines specific switching states required to produce various output voltage levels. By carefully selecting transformer turn ratios using finery algorithm geometric progression based on factor of 5 level inverter can generate 25 distinct voltage levels. This approach enhances voltage resolution and waveform quality, enabling finer control over an output and reducing total harmonic distortion (THD)

4. Modeling Photovoltaic Arrays and Maximizing Power Point Tracking Algorithm

Photovoltaic (PV) systems are capable of real-time dynamic operation, making them particularly suitable to energy management and grid incorporation requests. PV array typically consists of multiple modules, each containing several interconnected PV cells. In an associated diagram, I photovoltaic represents current produced by solar irradiance. PV equivalent circuit includes series and parallel resistances, denoted Rs and Rp, while I and V indicate output current and voltage of single PV cell.

Under standard test conditions irradiance with 1000 W/m² and cell temp with 25 °C output current of PV cell is described mathematically by Eq.

$$I = I_{photovoltaic} - I_{DS}\left[\exp\left(\frac{Q.V_{oc}}{A.K.Tm}\right) - 1\right] - \left(\frac{V + I.R_s}{R_p}\right)$$

IC method has become widely used because of its fast response and high accuracy. This method functions by comparing an incremental conductance (did/dB) with an instantaneous conductance (I/V) of a PV system; equality between these values indicates operation at a MPPA

A IC controller then modifies a switching duty cycle (DDD) to adjust a output voltage and maintain MPP operation. the schematic of a IC algorithm is provided in Fig. 8 [37].

Photovoltaic cells are highly sensitive to variations in both temperature and irradiance, which can directly affect their performance. In a relevant equation, Q represents an electron charge, IDS is a diode saturation current, K is a Boltzmann constant, nan denotes a diode idealist factor, and TMT_MTM indicates a PV cell's actual temperature.

5. Simulation Results

Here presents in-depth analysis of performance of hybrid SMC and PR control system integrated with MLI, applied to grid-connected PV system. performance of this advanced control system is examined under various fault conditions, including V sags, V swells, harmonic distortion, and G faults. system's ability to improve power quality, V regulation, and current tracking is evaluated. Additionally, performance of hybrid control system is compared with conventional control systems, such as PI controller and Linear control systems. simulation is conducted using MATLAB/Simulink, and such as voltage(V) deviation, current tracking accuracy, compensation efficiency are analysed.

5.1. Performance under Steady-State Conditions

Under normal operating conditions, with no faults or disturbances introduced, system performs as follows:

5.1.1. Current Regulation

The PR control maintains V at PCC within acceptable limits, preventing significant deviations. series inverter adjusts compensating V to stabilize G voltage. V at PCC remains within specified range, demonstrating effectiveness of hybrid control system.

5.1.2. Voltage Regulation

The PR control maintains V at PCC within acceptable limits, preventing significant deviations. series inverter adjusts compensating V to stabilize G voltage. V at PCC remains within specified range, demonstrating effectiveness of hybrid control system.

5.1.3. PV Power Injection under Normal Conditions

In normal operating conditions, system is expected to operate without disturbances. PV array generates power based on solar irradiance, which is then converted into AC power by inverter and fed into grid. UPFC ensures these both active and reactive power are effectively managed, maintaining stable V at PCC.

Figure shows variation in irradiance over time. MPPT system continuously tracks maximum power output from PV array. As irradiance changes 1000 W/m² to 250 W/m² and back to 1000 W/m², power injected into G adjusts accordingly, as shown in Fig 9(b).

Under these conditions, UPFC ensures these V stability is maintained at PCC by adjusting compensating V through series inverter. This stabilizes

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power injected into G, ensuring smooth and uninterrupted power flow. multi-level inverter further reduces harmonic distortion in output, ensuring clean and efficient power transfer to grid.

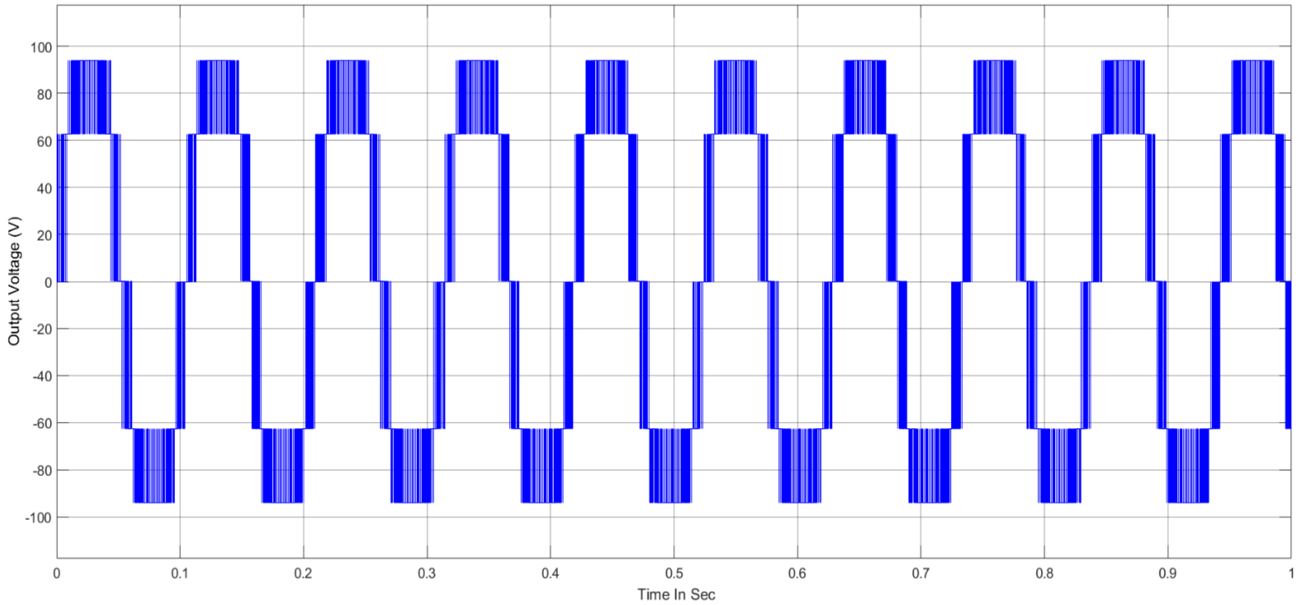

Figure. 8 Phase voltage of a multi-level inverter.

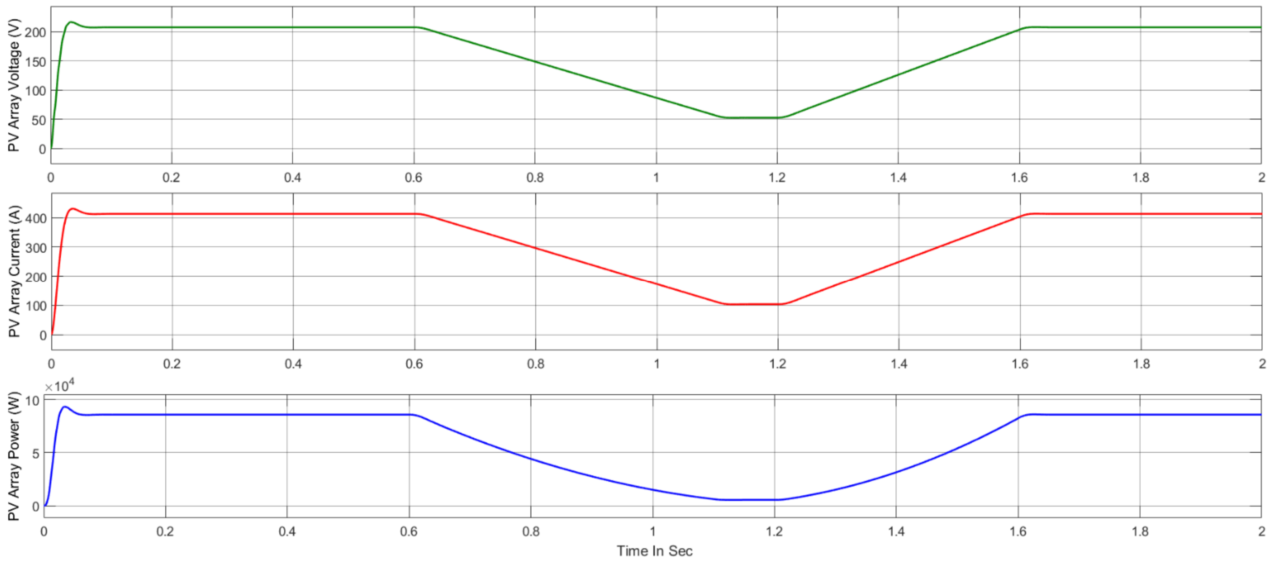

Figure. 9 Analyzing PV Power, PV Current, and PV Injection

5.2. *Voltage Sag*

A voltage sag is introduced at **t = 2 seconds** with the duration of 0.1 seconds. A system is evaluated on its ability to compensate for a voltage dip.

5.2.1. *Voltage Compensation a series inverter*

The **series** inverter detects the voltage sag and injects the compensating V to restore PCC Vto its nominal value. the hybrid control system reacts quickly to correct

5.2.2. *Current Regulation*

The shunt inverter, controlled by the SMC, ensures these the current injected into the grid follows the reference trajectory, even during the sag. the current tracking error remains low.

5.3. *Comparison with Conventional Systems*

In conventional systems, such as those using PI control, the compensation response is slower, leading to larger voltage deviations during the sag. the PI controllers may also introduce higher harmonic distortion during voltage sag recovery. the hybrid control system provides faster response times and superior voltage regulation.

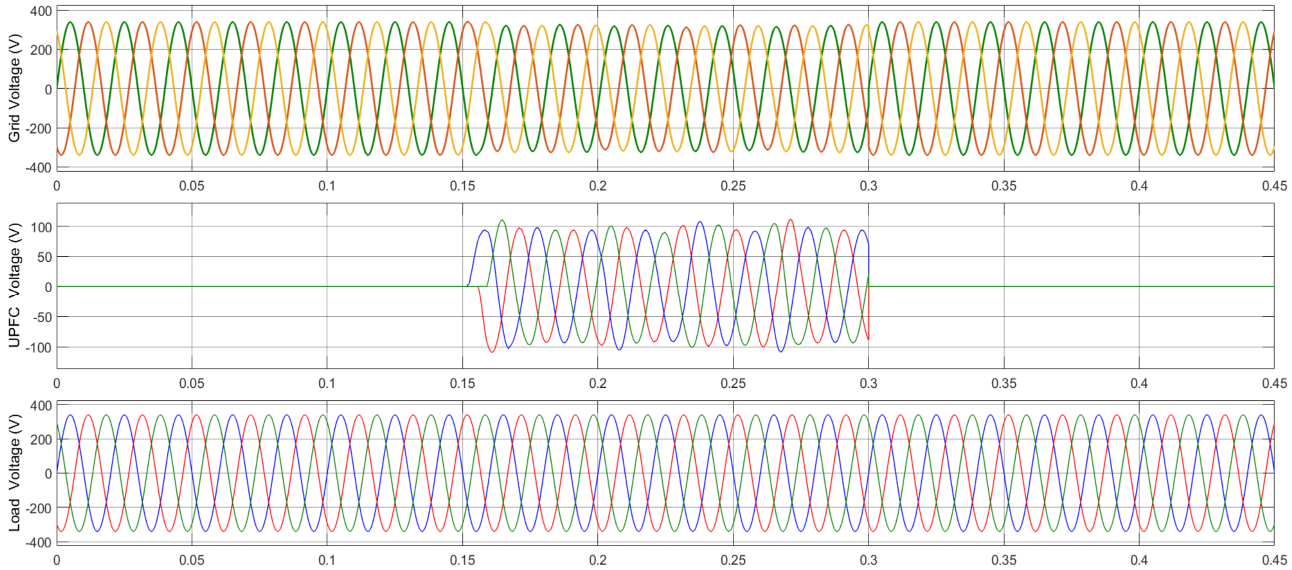

Figure.10 Steps in compensating for voltage drops (a) in the supply, (b) in the injection, and (c) in the load.

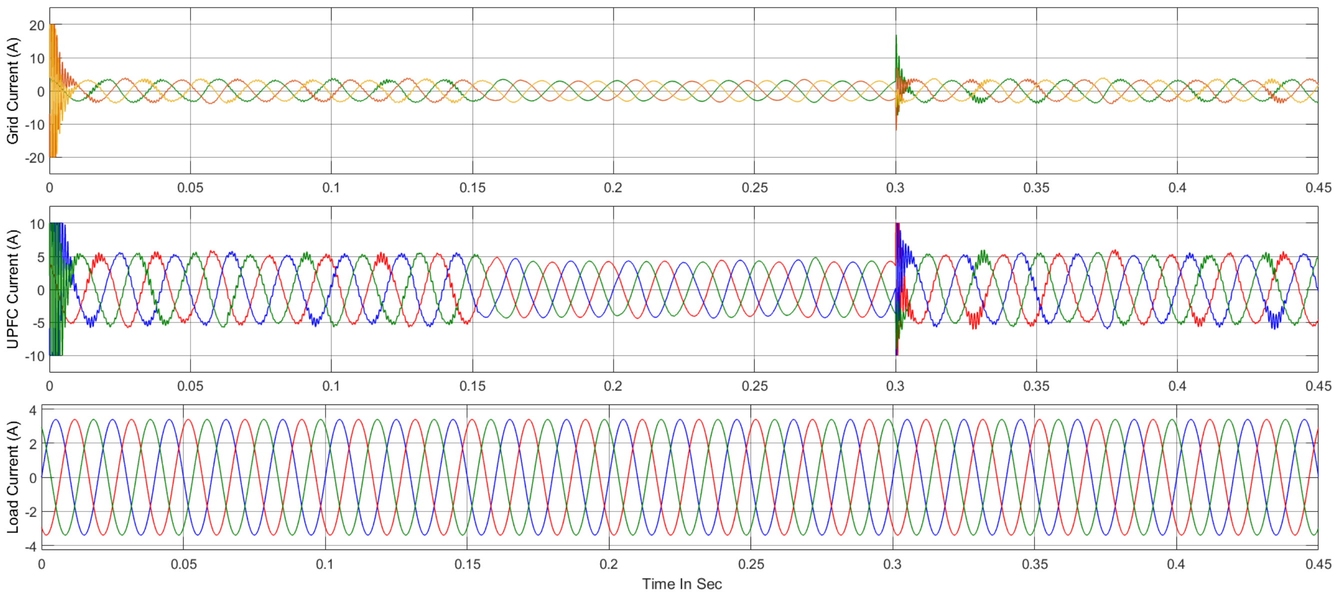

Figure.11 The three steps of compensating for a balanced current sag are (a) supply current, (b) injection current, and (c) load current.

5.4. *Voltage Swell*

A voltage swell is introduced at t = 0.15 s, lasting to 0.3 s, simulating situations such as load shedding or transients. As shown in Figure 17(a), the voltage increases significantly during the voltage swell event. An UPFC mitigates the swell by injecting the required voltage to stabilize the system. Figures 17(b) and 17(c) show how an UPFC restores the PCC voltage to normal levels by compensating to an overvoltage, ensuring a stable and reliable power supply to the grid.
A voltage swell is introduced at t = 0.15 seconds, lasting to t=0.3 seconds. the performance of the system under this condition is assessed.

5.4.1. *Voltage Mitigation*

The series inverter injects a counter-voltage to prevent the PCC voltage from exceeding the nominal voltage. the voltage at the PCC is restored to its nominal value within a few milliseconds

5.4.2. *Current Regulation*

The shunt inverter continues to regulate the current accurately, ensuring these an injected current remains close to the reference current.

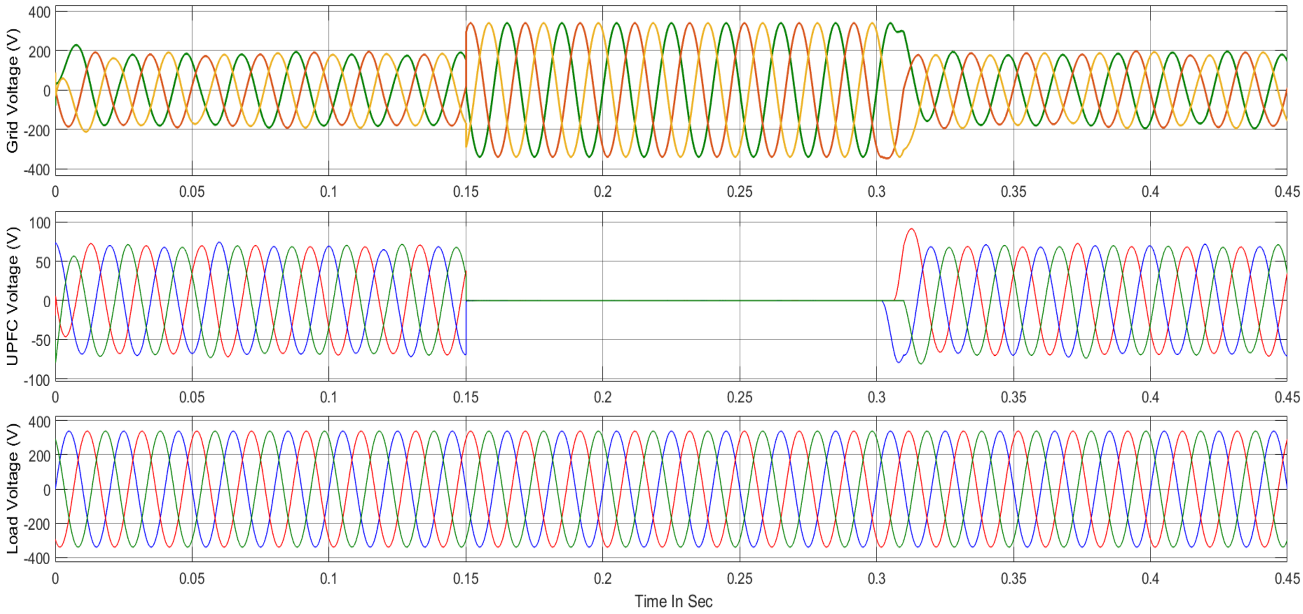

Figure.12 A technique for compensating for voltage spikes (a) Voltage supplied, (b) Voltage injected, and (c) Voltage applied to the load.

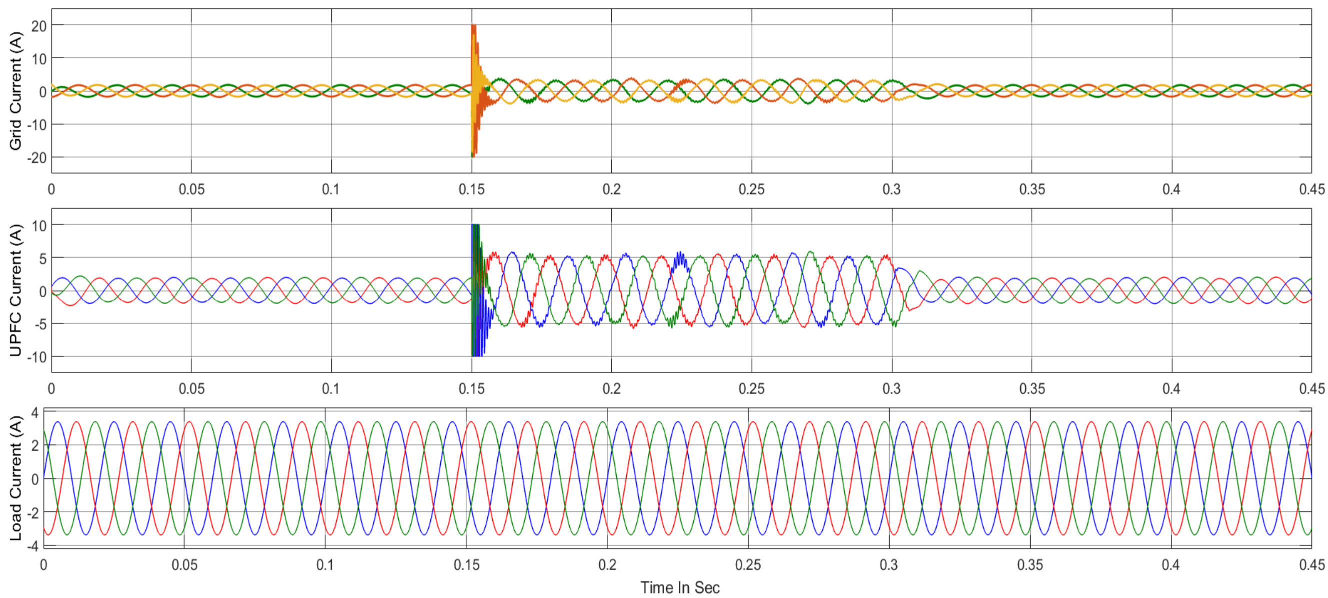

Figure.13 Balanced Current swell compensation process (a) Supply Current, (b) Injected Current, (c) Load Current.

5.5. Unbalanced Voltage Sag

Unbalanced voltage sag occurs due to faults these cause one or more phases to experience voltage dips. Figure 16(a) shows an onset of unbalanced voltage sag, which lasts from t = 0.15 s to t = 0.3 s. an UPFC compensates to an unbalanced voltage by vaccinating the required compensating V through series inverter, as illustrated in Figure 16(b). the PCC voltage remains stable during this period, as shown in Figure 16(c), with an UPFC successfully correcting the voltage imbalance and ensuring stable power delivery to the grid. This demonstrates an UPFC's capability to handle unbalanced voltage disturbances efficiently, ensuring these the system remains operational even during grid faults.

5.6. Unbalanced Voltage Swell

Unbalanced voltage swell is simulated from t = 0.15 s to t = 0.3 s, and an UPFC successfully compensates to an unbalanced voltage fluctuations. Figure 18(a) shows an unbalanced voltage swell occurring at the PCC, and Figure 18(b) illustrates the compensating voltage injected by an UPFC. the system continues to operate without significant disturbances, as evidenced in Figure 18(c), where the PCC voltage is kept within acceptable limits.

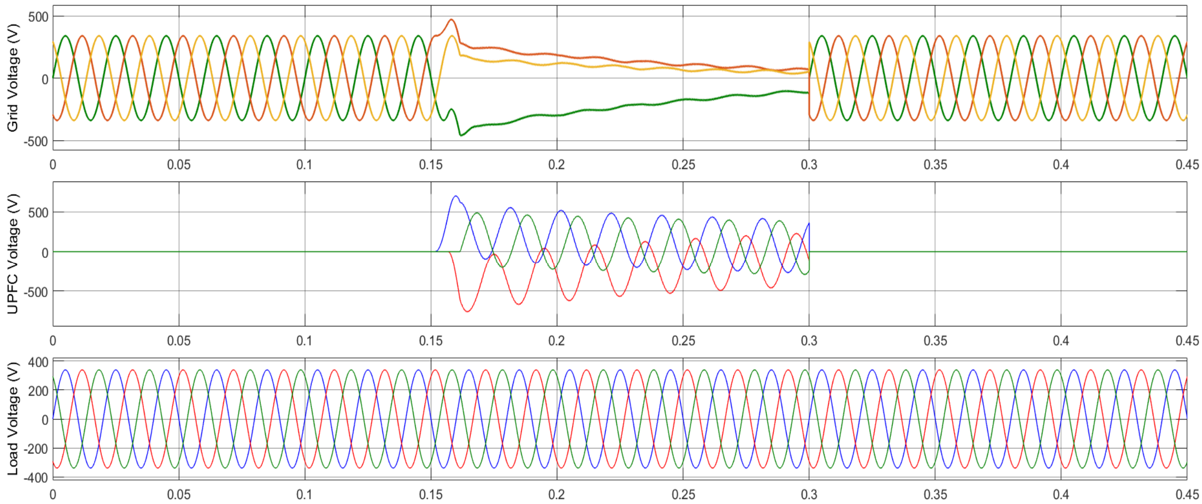

Figure.14 Unbalanced voltage sag compensation process (a) Supply Voltage (b) Injected Voltage (c) Load Voltage.

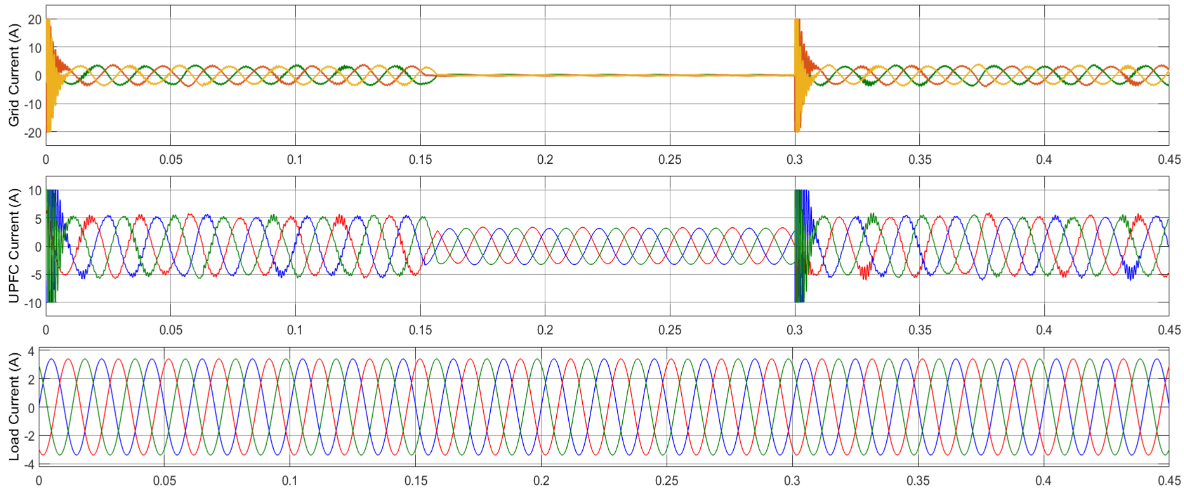

Figure. 15 Unbalanced Current sag compensation process (a) Supply Current (b) Injected Current (c) Load Current.

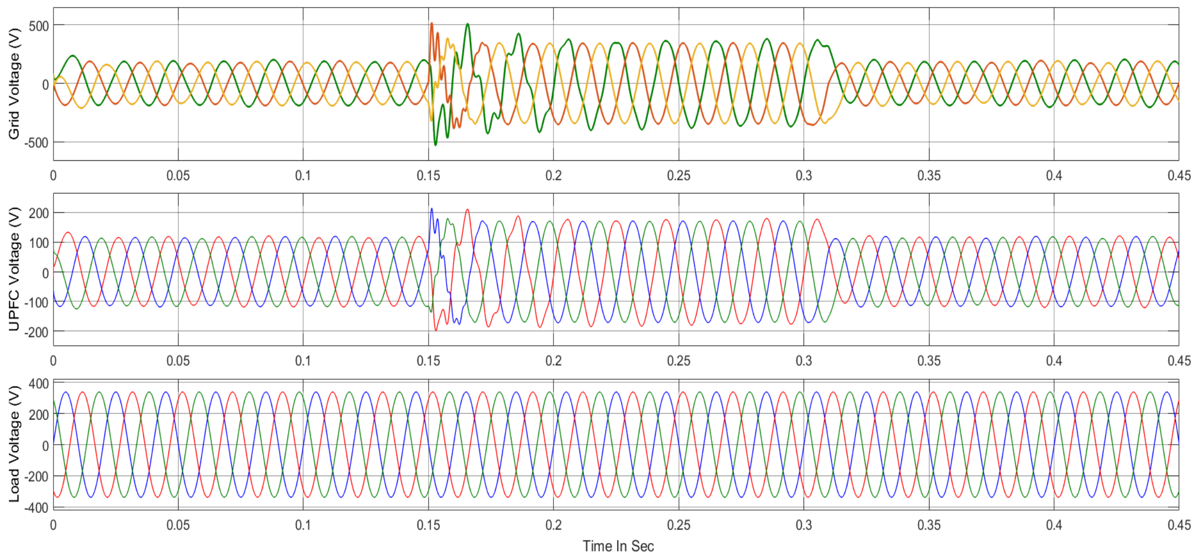

Figure.16 Unbalanced voltage swell compensation process (a) Supply Voltage, (b) Injected Voltage, (c) Load Voltage.

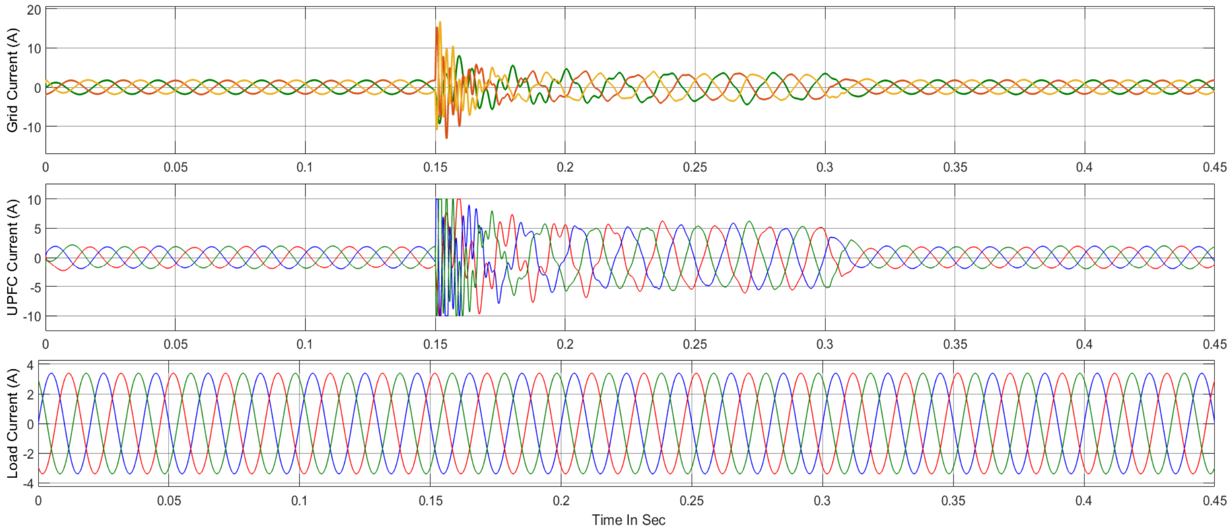

Figure.17 Unbalanced Current swell compensation process (a) Supply Current, (b) Injected Current, (c) Load Current.

6. Conclusion

The simulation findings show these grid-connected solar systems of multi-level inverter and the suggested hybrid control scheme these combines Sliding Mode and PR perform better than those without. By keeping a voltage and current levels steady, the system is able to efficiently reduce voltage dips, spikes, harmonic distortions. the fusion control system outperforms traditional systems in terms of reaction time, voltage regulation, and current tracking. Injecting voltage and current into the multi-level inverter guarantee quality power by reducing switching losses and harmonic distortion. the viable option to smart grid applications, a findings demonstrate these a suggested control method significantly improves power quality, voltage stability, and current regulation of grid-connected PV systems. Optimizing control algorithms to larger-scale PV systems and investigating real-time implementation and validation on hardware systems are potential areas to future research.

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