



Comparative Analysis of Advanced Shielding Techniques for Crosstalk Mitigation in Multi-walled Carbon Nanotube TSVs

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Abstract: This research introduces a novel method for reducing power consumption, crosstalk interference, PDP, and EDP in through-silicon vias (TSVs) based on multi-walled carbon nanotubes (MWCNTs) with polymer dielectric liners. The suggested TSV architecture makes use of bundles of multi-walled carbon nanotubes (MWCNTs) as conducting channels and insulating dielectrics made of low-k polymer liners, including polyimide, polypropylene carbonate (PPC), and benzo cyclobutene (BCB). A ternary inverter-driven coupled TSV's crosstalk behaviour is studied using an analogous electrical circuit model. At lower TSV heights in particular, simulation findings show that BCB-based TSVs outperform SWCNT TSVs by up to 30.21%. This improvement is based on data acquired using the HSPICE tool. Moreover, as compared to their SWCNT equivalents, TSVs coated with BCBs demonstrate superior crosstalk suppression throughout a larger range of TSV pitch values, providing an improvement of about 40.03% in the 0.5-3 μm pitch range. Additionally, the results show that compared to traditional SiO_2 liners, BCB reduces crosstalk latency by 43.8%. The findings show that polymer liners, particularly BCB, are a great alternative to next-gen 3D integrated circuit (3D-IC) technologies because they improve overall performance, decrease power loss, and greatly increase signal integrity.

Keywords: Crosstalk mitigation, MWCNT, PDP, SWCNT, TSVs.

1. Introduction

An impressive improvement in Very Large Scale Integration (VLSI) technology, three-dimensional integrated circuits (3D-ICs) provide many benefits, including a smaller system footprint, greater input/output (I/O) density, shorter connection lengths, and higher bandwidth [1]. Through-Silicon Vias (TSVs) are the backbone of this design, as shown in Figure 1. They allow for vertical integration by providing electrical channels across several stacked chip layers [2]. With these vertical connections, it's possible to improve performance and functionality by integrating disparate systems on one platform. The usual building blocks for TSVs include conductive materials like polysilicon, copper, tungsten, or composites of metallic polymers. Because of its high thermal and electrical conductivity, copper is still the material of choice among these [3]. Despite these advantages, 3D-IC systems' long-term stability and performance might be affected by reliability issues with Cu-based TSVs, such as electromigration, increased resistivity, and signal integrity deterioration [4].

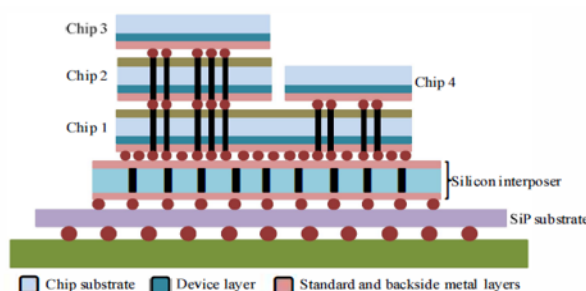


Figure.1 3D Architecture

Graphene nanoribbons (GNRs) and carbon nanotubes (CNTs) are two examples of the new interconnect materials that researchers are using to overcome the limitations of traditional copper-based through-silicon vias (TSVs). In particular, carbon nanotubes' (CNTs') remarkable electrical and thermal characteristics have attracted a lot of attention. There are two main forms of carbon nanotubes, which have different uses for nanoscale interconnects: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). They are ideal for use in TSVs because of their outstanding mechanical, electrical,



and thermal qualities. Because of its superior current-carrying capability and easier production procedure, MWCNTs are highly favoured among them [5]. To keep signals intact in TSVs, it is critical to choose a suitable dielectric liner in addition to the conductor material [6]. The crosstalk effects are magnified by conventional silicon dioxide (SiO_2) liners, which have a tendency to increase coupling capacitance [7].

Several low-dielectric-constant (low-k) polymers, including polyimide, benzo cyclobutene (BCB), and polypropylene carbonate (PPC), have been suggested as potential solutions to this problem by successfully reducing capacitive coupling. A similar electrical model for CNT-based TSVs, taking into account capacitive and conductive interactions inside the silicon substrate, is also presented in this study.

Under varying switching circumstances, the signal integrity and crosstalk delay of Cu-, SWCNT-, and MWCNT-based TSVs are evaluated in detail [8]. These findings point to CNT-based TSVs as a potential replacement for traditional Cu interconnects in high-end 3D-IC systems due to their enhanced power efficiency, signal propagation, and bandwidth. [9].

Table.1 The dielectric constant of SiO_2 and polymer liners differs depending on their material composition and properties.

Dielectric insulators	Dielectric Constant
Silicon Dioxide	3.9
Polyimide	3.5
polypropylene carbonate	2.9
Benzo cyclobutene	2.65

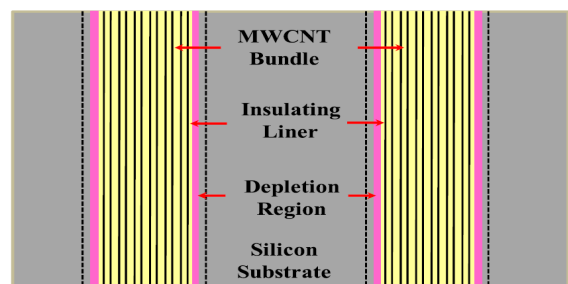
Various dielectric liners exhibit relative permittivity variations, as seen in Table 1. Silicon Dioxide has a relative permittivity of 3.9, polyimide of 3.5, polypropylene carbonate of 2.9, and benzo cyclobutene of 2.65. whether you want to know how well insulation works or whether a material is good for high-frequency uses, you need to know its dielectric characteristics.

New TSV designs using MWCNTs as conductors and dielectric liners made of polymers are suggested in this study. Accurate and trustworthy performance analysis is achieved by conducting thorough evaluations of the suggested circuits using the widely-used HSPICE simulator.

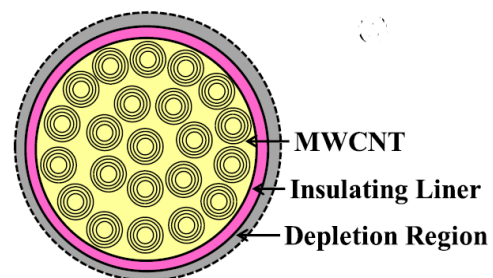
They are tested against standard TSV designs to find ways to improve performance and their electrical behaviour, particularly with respect to crosstalk, is studied in detail.

2. Structure and Corresponding Electrical Model

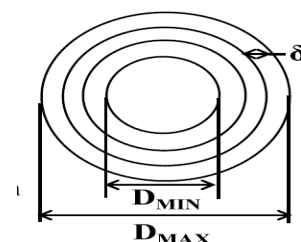
For the suggested MWCNT-based TSV structure with polymer dielectric liners, this part kindly presents the electrical equivalent circuit model. In comparison to traditional TSV arrangements, the use of low-k polymer liners and multi-walled carbon nanotubes (MWCNTs) significantly lowers coupling capacitance in nearby TSV lines. This kind of integration improves connection efficiency, signal integrity, and the reduction of crosstalk. As a result, using MWCNTs in coupled TSV structures is an exciting new direction for 3D-IC designs that aim to optimize signal transmission while improving electrical isolation.



(a) Physical configuration of the TSV



(b) Top-Down View of TSV Elements: Spatial Arrangement and Distribution



(c) Structural Alignment and Conductive Pathways of MWCNT Bundles in 3D-IC Designs

Figure.2 shows the proposed MWCNT-bundled Through-Silicon Via (TSV) architecture, providing a detailed visual of its structural design.

Subfigure (b) provides a top-down view of the spatial arrangement and distribution of TSV components. In contrast, subfigure (c) focuses on the MWCNT bundle, emphasising its structural alignment

and conductive network that improve electrical performance and reduce crosstalk in advanced 3D-ICs.

According to the schematic, the MWCNT bundle is the principal conduction medium, and the insulating dielectric material around it prevents current leakage and minimizes crosstalk. In order to guarantee steady functioning, the insulating layer separates the current-carrying area from the depletion zone. Substrate qualities, charge concentration, and applied bias voltage are a few of the variables that influence the depletion layer's density and extent. Figure 3 shows the result of developing an electrical model of the TSV that is identical to this setup.

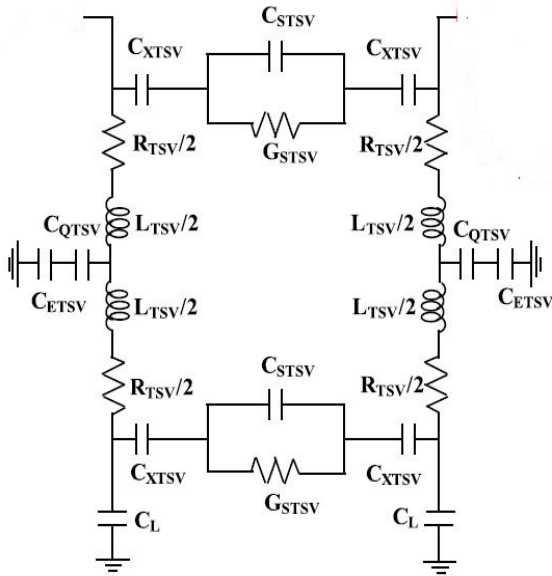


Figure.3 Electrical analogous representation or circuit model of MWCNT-based TSVs.

As shown in Fig. 3, $R_{TSV/2}$ stands for resistance, $L_{TSV/2}$ for inductance, C_{QTSV} for quantum capacitance, C_{ETSV} for electrostatic capacitance, C_{STSV} for substrate capacitance, G_{STSV} for substrate conductance, and C_{XTSV} for the TSV's insulating capacitance.

Defects, acoustic phonon dispersion, static impurity scattering, and line-edge roughness are among the causes of R_{TSV} resistance. The suggested MWCNT-bundled TSV's R_{TSV} is calculated as

$$R_{TSV} = R_{QTSV} \left(N_{[MWCNT]} \sum_{j=1}^{j=n} N_{ITSV} \lambda_{ITSV} \right)^{[-1]}$$

The R_{QTSV} , N_{MWCNT} , N_{ITSV} , and λ_{ITSV} are the quantum resistance, the overall number of conducting pathways within the MWCNT bunch, the number of active channels in the j th shell, and the electrostatic mean free path of the j th shell, respectively. These elements are all important in the system. The suggested MWCNT-based TSV's

inductance (L_{TSV}) is a result of both dynamic (L_{KTSV}) and magnetism contributions. The suggested TSV structure provides the following equation for L_{TSV} .

$$L_{TSV} = \log_{TSV} + \frac{L_{KTSV}}{N_T}$$

$$L_{KTSV} = \frac{\mu \epsilon_0}{C_E h}$$

$$L_{KTSV} = \frac{\mu \epsilon_0}{4e^2 N_T V_{fr}}$$

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$$C_E = \frac{6.28 \epsilon_0 \epsilon_{SiO_2}}{\cosh^{-1} \left(\frac{0.5 D_{WCNT} + D_{GAP}}{0.5 D_{MWCNT}} \right)}$$

The total number of conducting channels inside the TSV is represented by N_T in this context, whereas the permeability and permittivity of empty space are μ_0 and ϵ_0 , respectively. V_{fr} stands for the Fermi velocity, h for Planck's constant, and e for the elementary charge.

A parameter representing the permittivity of silicon dioxide is ϵ_{SiO_2} . On the other hand, $DMWCNT$ stands for MWCNT length and D_{GAP} for distance between MWCNT bundle and neighboring conductive plane. The quantum capacitance is denoted as C_{QTSV} in the suggested equivalent circuit model, whereas the electromagnetic capacitance of the TSV structure is represented by C_{ETSV} . The following are the mathematical expressions of the parameters.

$$C_{QTSV} = \frac{N_T e^2}{h V_{fr}}$$

$$C_{ETSV} = \frac{6.28 \epsilon_0 \epsilon_{SiO_2}}{\cosh^{-1} \left(\frac{D_{GAP}}{D_{MWCNT}} \right)}$$

3. Simulation Results and Discussion

The predicted ternary-logic MWCNT-based TSV architectures with various insulating lining materials are investigated in this part, along with the interactions among power dissipation, power delay product, energy delay product, and crosstalk-induced noise.

It also delves into the ways in which these crucial performance metrics are affected by variations in TSV height. To further evaluate the efficiency and signal-integrity properties of MWCNT- and SWCNT-based TSV designs, a comparison research is also performed.

In the coupled TSV configuration, the main TSV serves as the aggressor, while the adjacent TSV acts as the victim. The proposed TSV design operates at a supply voltage of 0.9 V with a termination load of 0.1 fF. Crosstalk effects resulting from switching activities are classified into two categories: functional crosstalk and dynamic crosstalk. Functional crosstalk occurs when the switching of the aggressor TSV alone induces a voltage disturbance in the victim TSV. Conversely, dynamic crosstalk takes place when both TSVs switch simultaneously and can be further categorised into in-phase and out-of-phase delays. In-phase delay arises when both TSVs switch in the same direction, while out-of-phase delay occurs when they transition concurrently but in opposite directions.

The HSPICE program is used to simulate the proposed MWCNT-based linked TSV structures in order to conduct a thorough analysis of these interactions. Functional and dynamic crosstalk behaviour, power dissipation patterns, and important performance metrics, such as the power-delay and energy-delay products, are all thoroughly illuminated by this simulation. Enhancing signal integrity and overall connection efficiency in modern 3D-IC systems, the results lead to the development of optimized TSV design approaches.

3.1. Functional Crosstalk

Figure 4 shows how inverter-logic TSVs based on MWCNTs behave when subjected to functional crosstalk with varying insulating liners and TSV heights. The results show that compared to SiO₂, polymer liners significantly reduce noise levels. This is mainly due to the fact that polymers have a lower dielectric constant, which helps to reduce interference from undesired signals.

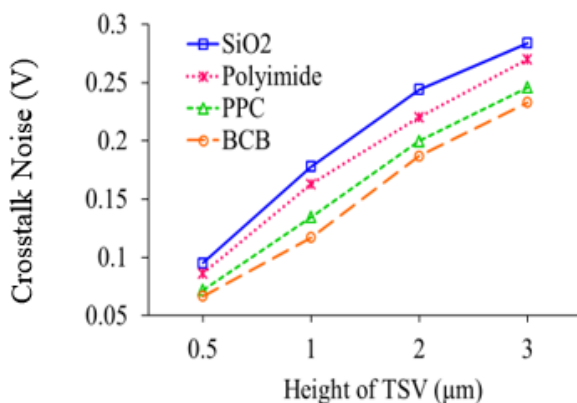


Figure.4 Crosstalk noise waveform

In addition, the effect of structural dimensions on signal integrity is shown by the fact that noise levels tend to rise with increasing TSV height. The advantages of polymer-based insulation are shown in Fig. 4, which shows the

noise waveforms for inverter logic MWCNT TSVs with SiO₂ and BCB liners at a 3 μm TSV height.

3.2. Dynamic Crosstalk

It occurs when both the aggressor and victim TSVs switch simultaneously, impacting signal integrity. It is classified into in-phase and out-of-phase delays. In-phase delay occurs when both TSVs transition in the same direction, resulting in synchronised signal propagation. Conversely, out-of-phase delay occurs when the TSVs switch in opposing directions, leading to increased interference and potential degradation of signal fidelity. The intricate interplay between these switching dynamics underscores the critical role of TSV configuration in mitigating crosstalk-induced distortions.

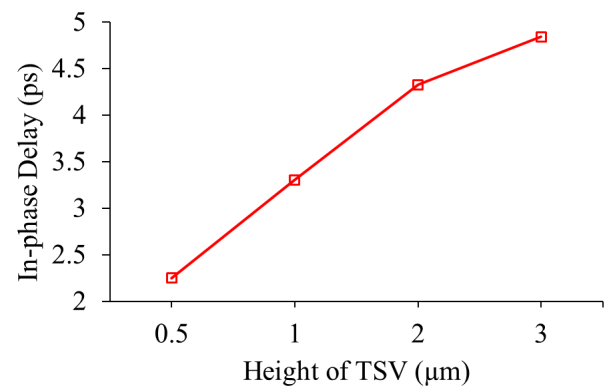


Figure.5 Dynamic crosstalk in-phase delay.

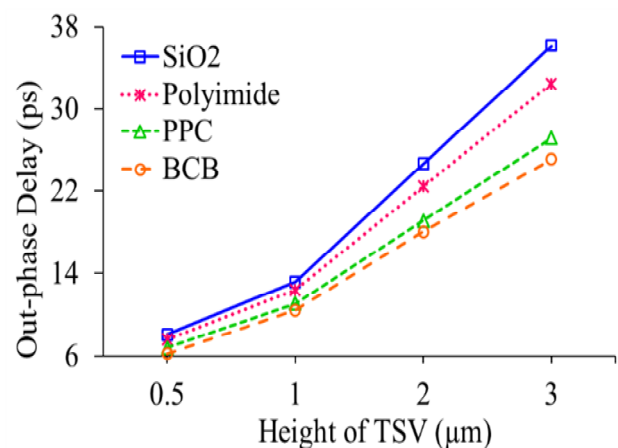


Figure.6 Dynamic crosstalk out-of-phase delay

For different TSV heights, Fig. 5 shows the in-phase delay properties of the suggested TSVs with SiO₂ liners. This study highlights the effect of structural dimensions on signal propagation by showing that longer in-phase delays are directly correlated with higher TSV heights. At the same time, the out-of-phase delay trends are shown in Fig. 6, which demonstrate a significant decrease when polymer liners are used instead of SiO₂. Polymer materials' reduced

coupling capacitance, which reduces signal interference and increases transmission efficiency, is largely responsible for this improvement.

Power Dissipation: Evaporation is the process by which electrical energy is converted into heat by use of capacitance, switching, and resistance. Factors including dielectric material, coupling capacitance, and TSV height affect power dissipation in TSV-based interconnects.

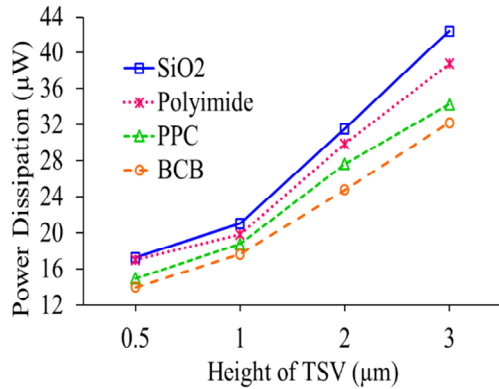


Figure.7 illustrates the power dissipation of TSVs as a function of height for different dielectric liners.

Because of its higher dielectric constant, SiO₂ has the largest power dissipation. On the other hand, polymer liners like BCB, PPC, and polyimide considerably lower power loss. Power dissipation increases for all materials as the TSV height grows, with the gap between the polymer liners and SiO₂ expanding the most. Based on its low power dissipation, BCB stands out as the top choice for high-performance applications that want to minimize energy loss.

3.3. Power Delay Product

Various dielectric liners, such as SiO₂, polyimide, PPC, and BCB, show the fluctuation of PDP via TSV height in Fig. 8. Because of its greater dielectric constant, SiO₂ has the greatest PDP, which rises as the TSV height does as well.

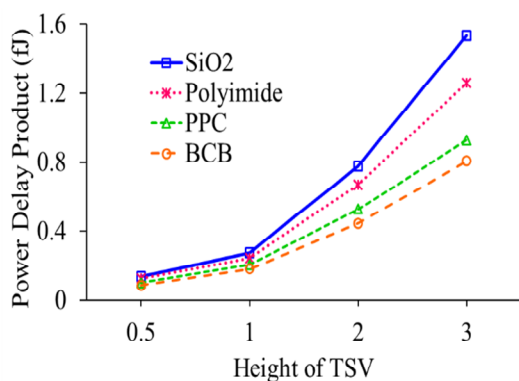


Figure.8 Variation of Power Delay Product (PDP) with TSV height for different dielectric liners.

Liners made of polymers, including BCB and PPC, have a lower PDP, which means they are more energy efficient.

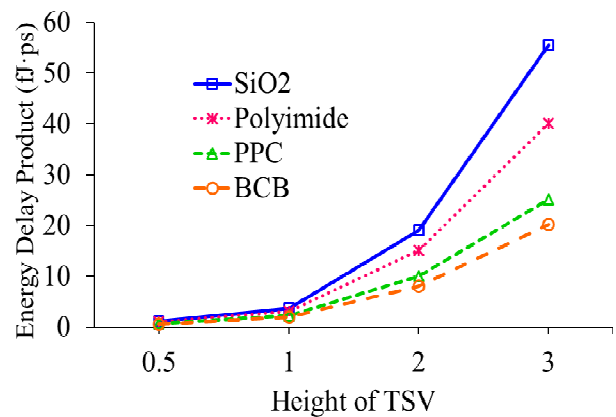


Figure.9 Variation of Energy Delay Product (PDP) with TSV height for different dielectric liners

This pattern emphasizes how choosing the right dielectric material may cut down on power usage and latency in TSV-based connections.

3.4. Energy Delay Product

Fig.9 presents the variation of Energy Delay Product (EDP) with TSV height for different insulating liners, including SiO₂, polyimide, PPC, and BCB. It is observed that EDP increases with TSV height, with SiO₂ exhibiting the highest values due to its higher dielectric constant and associated parasitic. Polymer-based liners, such as BCB and PPC, exhibit lower EDP, indicating better energy efficiency and faster performance. This trend highlights the importance of choosing appropriate dielectric materials to optimize TSV-based interconnect performance.

Table.2 Performance assessment of MWCNT-based TSVs using various insulating liners.

Evaluation Criteria	SiO ₂	Polyimide	PPC	BCB
Maximum Interference Noise(V)	0.284	0.270	0.246	0.233
Out-phase Delay (ps)	36.18	32.49	27.12	25.06
Power Consumption (μW)	42.36	38.71	34.22	32.19
PDP (fJ)	1.53	1.25	0.92	0.80
EDP (fJ.ps)	55.46	40.08	25.17	20.22

Table 2 presents the final performance parameters of dielectric liners, showing that BCB exhibits the lowest peak

crosstalk noise (0.233 V), out-of-phase delay (25.06 ps), power consumption (32.19 μ W), PDP (0.80 fJ), and EDP (20.22 fJ.ps). These results highlight BCB's efficiency in reducing power and delay.

4. Conclusion

Since current systems have smaller noise margins than previous generations, crosstalk has emerged as a major issue in logic circuit design as a result of the continuing advancements in semiconductor technology. Using various polymer dielectric liners, this work analyses and compares functional and static crosstalk, power dissipation, Power-Delay Product (PDP), and Energy-Delay Product (EDP) in quaternary logic MWCNT-based TSVs. Improving signal integrity and overall circuit performance may be achieved by using polymer liners with low dielectric constants. These liners efficiently minimize coupling impedance between neighbouring TSVs. Based on SPICE simulation findings, MWCNT TSVs lined with BCB outperform those without the liner when compared to other insulating materials. Integrated circuit manufacturers still choose Polypropylene Carbonate (PPC) over BCB as a liner because of PPC's superior adhesion, high fluidity, consistent surface quality, and structural flexibility, even though BCB is the best liner for reducing interference and improving electrical performance. A dielectric for next-generation semiconductors and 3D-ICs, PPC has all the right stuff.

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