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Design and Implementation of BIST Architecture for Low Power Applications using VERILOG

K Sai Venu Prathap [1*], A Anil Kumar [2], K Murali [3], S Guru Murthy [4], B Hemanth Kumar [5]

[1*,2,3,4,5] Department of Electronics and communication, Jawaharlal Nehru Technological University Anantapuramu, (JNTUA), Andhra Pradesh, India

** Corresponding Author: K. Sai Venu Prathap; venu.mits@gmail.com*

Abstract: In Now-a-Days we have more demand the Low power VLSI application. To design we are implementing of Built-In Self- Test (BIST) architecture using Verilog. We are proposed BIST architecture, in focuses on minimizing power consumption during the testing phase while maintaining high fault coverage. It leverages the capabilities of the Verilog hardware description language to model and simulate the design. The Project investigates various power reduction techniques, including test pattern compression, selective clock gating, and power-aware test scheduling, ta optimize power consumption during testing. Our project presents the design and implementation of a BIST architecture specifically tailored for low-power Very Large Scale Integration (VLSI) Applications. By implementing FPGA (Field programmable gate array) boards demonstrating the feasibility and practicality of the proposed design. The increasing demand for energy-efficient electronic devices and the proliferation of portable systems have necessitated the development of power-aware design techniques, BIST, a on chip testing technique, plays a crucial role in ensuring the quality and reliability of integrated circuits. The findings from this study can guide designers in developing energy-efficient and reliable integrated circuits, promoting sustainability, and extending battery life in portable devices. The proposed design is compatible with standard Verilog synthesis and is readily applicable to a wide range of low-power VLSI applications. This project presents a comprehensive study, design and implementation of a BIST architecture tailored for low-power VLSI applications, leveraging the Verilog hardware description language.

Keywords: BIST,FPGA, ATPG, Clock Pulses, RTL Schematic, Power.

1. Introduction

Built-In Self-Test (BIST) is a method used to automate the testing of integrated circuits (ICs) and electronic systems. Rather than relying on external testing equipment, BIST integrates self-contained testing mechanisms directly into the circuit or system during the design phase. BIST empowers circuits or systems to self-test, freeing them from reliance on external equipment. It integrates essential testing components directly into the design, including pattern generators and response analyzers. These structures autonomously generate test patterns, apply them, and analyze responses, streamlining and enhancing the testing process. BIST offers testing flexibility for circuits or systems, supporting functional, parametric, and structural tests as needed. Its adaptable structures allow for testing adjustments without major modifications, ensuring effectiveness even with design updates. While currently confined to machine-based processes, there's potential for future expansion into hardware verification within the VLSI domain. This adaptability enhances the verification process across different units, hinting at future possibilities for hardware advancements. BIST detects circuit faults, including manufacturing defects and design flaws, by embedding testing capabilities within the system. This internal testing reduces time and costs associated with external procedures, enabling swift fault identification. It streamlines the overall testing process, enhancing efficiency and reliability. BIST finds application in diverse electronic systems, spanning microprocessors, memory modules, ASICs, and complex integrated circuits. Its integration within these systems facilitates thorough testing, enhancing reliability and quality assurance.

By enabling comprehensive testing directly within the system, BIST plays a pivotal role in identifying and addressing issues early in development or manufacturing. This proactive approach helps prevent potential failures in real-world applications, bolstering overall

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performance and longevity. The project "Design and Implementation of BIST Architecture for Low Power Applications using Verilog" aims to develop a tailored Built-In Self-Test (BIST) system for Very Large Scale Integration (VLSI) circuits with a primary goal of minimizing power consumption. Verilog, a hardware description language, is utilized for both design and implementation. The project involves crafting a specialized BIST architecture specifically suited for VLSI applications. This architecture is engineered to autonomously conduct tests on the integrated circuits within the VLSI system, guaranteeing robust functionality while prioritizing low power consumption.

2. Literature Survey

The innovative methodology dynamically alters the seed value every two cycles, employing an m-bit counter and gray code generation for efficient modulation. This approach exhibits high fault resistance, showcasing robust fault-tolerant traits. By dynamically adjusting the seed value, the technique enhances test coverage, proficiently detecting diverse faults within the 32-bit multiplier circuit. The implemented BIST scheme integrates signature analysis using multiple registers to capture and evaluate distinctive signatures during testing. These signatures indicate circuit integrity, enhancing reliability and accuracy. With dynamic seed value modulation, fault resistance, and signature analysis, the low-power BIST technique for the 32-bit multiplier ensures thorough and dependable testing.

The novel methodology prioritizes time efficiency and high-grade output verification for complex System-on-Chip (SoC) designs. It effectively addresses challenges associated with verifying modern integrated circuits, notably reducing verification time without compromising quality. This approach stands out for its efficiency in handling the verification process of intricate SoC designs, offering a solution to the growing complexities in integrated circuit verification. The methodology addresses the time efficiency needs of modern SoC designs, tailored for complexity and scale. It offers a comprehensive verification approach, ensuring thorough validation of diverse SoC components and functionalities, including performance, security, and compliance.

D S Kirthi proposed the seed value at regular intervals of precisely every clock pulses and data functions the output of counter processed in gray code generation. In the Pseudo Random pattern Generator by automatically generating by input themselves only. In that place we can place any switch ,LFSR any types of working device.

E.H Yuejain had proposed the Built in functional test for silicon validation and system integration of System on chip design. we can exhibit concurrently achieving high grade output verification for the multifaced designs of system on chip.

Vivek Hadge proposed the test pattern generation algorithm with the name as D Algorithm towards enhanced in fault detection within digital circuits. we can simply compare into detection of critical faults like struct at 0, struct at 1 and short faults.

Bharathi Misra proposed the test pattern generator of design to produce random 4 bit numbers for testing. It is sharing of bit to bit ratio we can this method by using of xilinx vivado software.

Michal Filipek proposed the low power test pattern generator. This can be integrating seamlessly with scan shift in switching. The hybrid solution presented the logical BIST, providing a comprehensive solution that balances the need for optimized test patterns with the demand for through fault coverage.

3. Proposed Method

BIST automates functionality verification in machines by generating tailored patterns through specialized algorithms for circuitry or defects. Various implementations of the comparison function, utilizing signal detectors with comparators, demonstrate its versatility. This project emphasizes Memory BIST (MBIST) development, employing algorithms tailored for identifying and rectifying memory-related flaws.

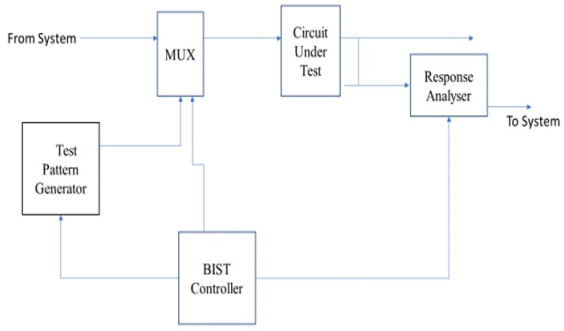

Fig.1 Circuit with surrounding built-in self- test circuitry

At first of all, for MUX we are taking the inputs from system and test pattern generator and 1 selection line as test mode, after the output of MUX it passes one output to the CUT(Circuit Under Test) in that we are placing the full adder at the final of output response we are taking the 4 bit LFSR the output can be observed in different parameters. A meticulous testing strategy based on 1024 inputs with

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32-bit data each will be implemented. A detailed test bench using Model Sim will be crafted to demonstrate stuck-type fault models and systematically generate patterns for read-and-write operations. In this complex testing scenario, the memory model and BIST controller take center stage. The memory model accurately simulates real memory behavior, providing a platform for testing various fault models. Meanwhile, the BIST controller acts as a vital orchestrator, overseeing test procedures, executing patterns, and assessing the memory's responses. Together, these components form the backbone of the testing framework, ensuring thorough evaluation and validation of memory functionality.

3.1. Manufacturing of Test of IC

In integrated circuit (IC) manufacturing, comprehensive tests are essential to detect and rectify fabrication irregularities before delivering finalized circuits. These tests identify physical flaws like shorts or opens, crucial for maintaining circuit integrity. They play a pivotal role in ensuring reliability and performance, meeting stringent industry standards before products reach customers.

Post-manufacturing fault diagnosis is crucial for identifying root causes of defects, facilitating refinement of manufacturing procedures to enhance quality and reliability. This iterative process accelerates learning curves for improving yield rates and refining IC batches.

Functional testing is effective for evaluating memory cores, but simultaneous malfunctions, particularly interconnected faults, pose challenges. Understanding how faults interact is crucial for developing robust testing strategies that accurately assess memory core resilience. These faults are commonly found in machines, keyboards, switches, and logical connections in everyday life.

Fault Combinations

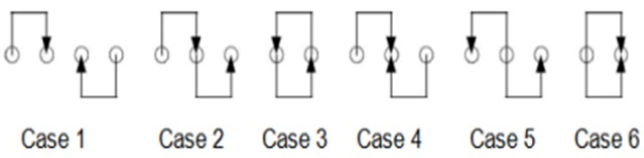

Fig .2 Two Coupling Faults

4. Existing Method

BIST is a self-testing of any device before it is working in any device. It enhances the capability of the digital testing blocks of testing means verification of any unit specifically.

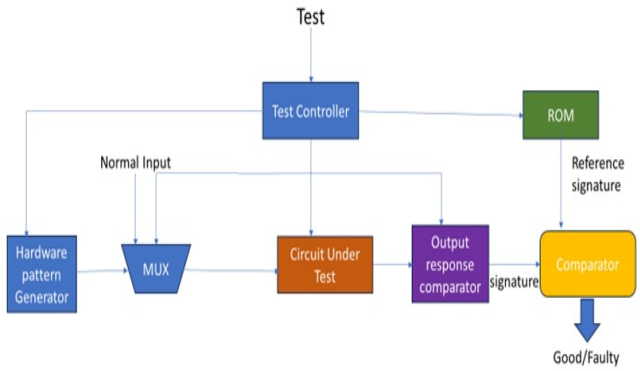

Fig.3 BIST Architecture

4.1. Explanation

As we shown the above figure BIST Architecture, we are testing an IC in our project testing means verification of a unit it must be related to the electronic device.

In the test controlling we are generating a 3 bit LFSR, it combines the full adder in the CUT, with MUX decides the output of any one of output here we have 1 selection line is in test mode.

It compares the given data into the comparator to resultant output data is good/faulty.

In this project we are implementing the 3 blocks TPG (Test Pattern Generator), CUT (Circuit under test with full adder), Output response with the 4 Bit MISR.

We are implementing the Verilog code in the Xilinx vivado tool with version 2018.3version with the outputs of the various parameters in the results.

Here the project summary consists of the FPGA Board of Artix 7 with the CPG 236 Packages. We know that the FPGA is a type of boards with the interconnection of cells in the series and in parallel.

Here Artix 7 produces the 10,400 Slice LUTs, Here in this project we need only 8LUTs. 6 for BIST and 2 for Test pattern generator.

The parameters of the Power produces the 8 W, Delay of 5 seconds with the schematic diagram of RTL and the technology schematics RTL is based on the coding and Technology is based on the LUTs.

5. Results

This project finds that the simulation wave form of the BIST Architecture of clock pulses, reset, input selection lines, test mode, full adder, MUX, LFSR & MISR of their

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respective behaviour in various modes.

Here the clock is the timing pulses of the logic 0 and logic 1 respectively, upto infinite. The timing of the clk pulses are in the nano seconds.

Reset is the ideal statement that initially starts from high i.e.., logic 1 after operating mode it turns to 0.

Every output of the graph starts from Positive Edge of the Clock pulses.

From the Fig, w, x, y are the input of the full adder and observes the sum=1 & carry=1.
The full adder output is in 3 bit mode, because it is concatenation of sum and carry, it means combination of sum& carry.

Here the MUX is 2:1, we know that the mux is combinational circuit with 2^n inputs and only 1 output only, n is referred to number of selection lines, According to our project here n is in test mode operation and the 2 inputs are input from test pattern generator& the system.

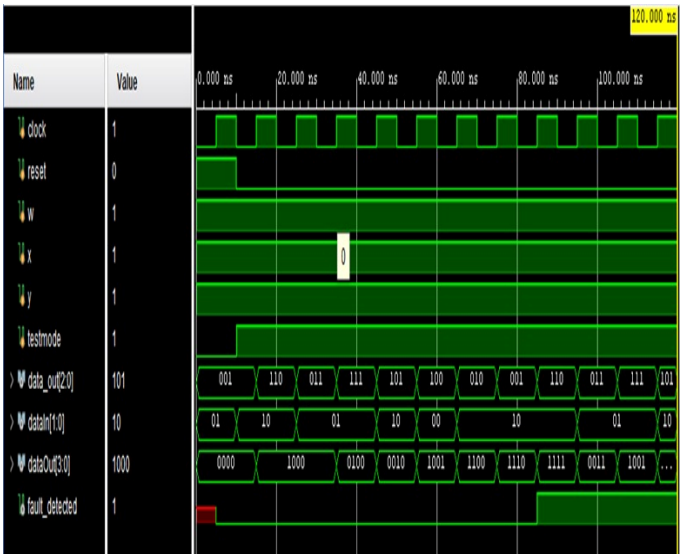

Fig.4 Simulation waveform of BIST

Data of the LFSR is in 4 bit, it is a combination of the next state equation upto counting of less than 6 in the given input LFSR code.

The Data of the MISR of the golden signature of “0100” from the testbench, it is not obtained in the MISR output. So, Hence it is an error of getting a fault, As we are proving the Digital testing that is good/faulty that is observing here.

The logic 0 implies that absence of faults and logic 1 implies that presence of faults, hence 0110 is not in MISR Output, Hence it is faulty that is from an IC.

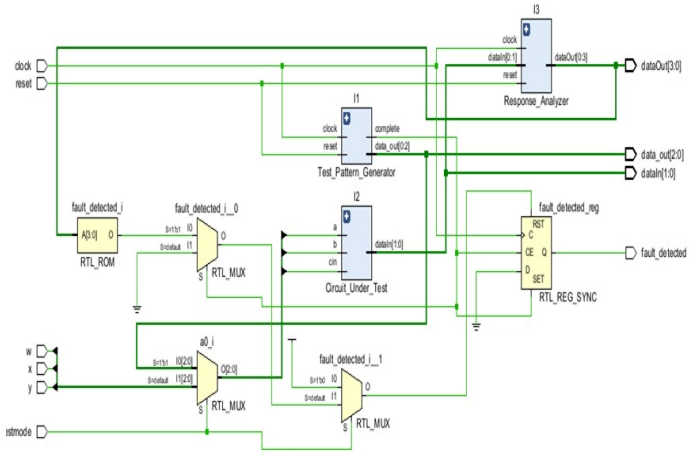

Fig. 5 RTL schematic of BIST

The RTL schematic diagram of BIST is the clean explanation of the input portable pins with the clock, reset, test mode, w, x, y, a, b, c, mux, CUT, Test pattern generator, ROM.

Based on the selection line, RTL schematic is the based on code generating form.

These all pins are portable and clear connection all connections.

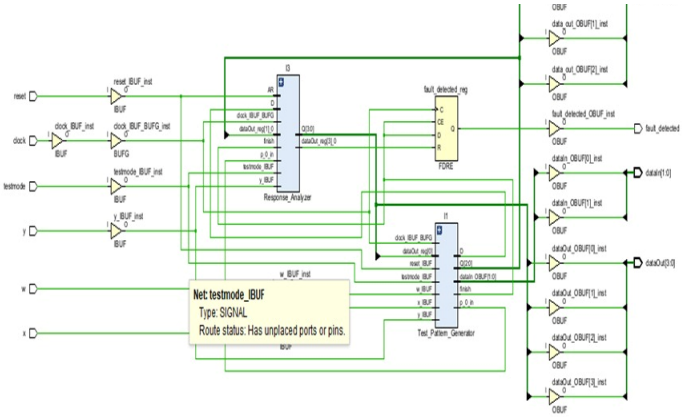

Fig.6 Technology schematic of BIST

It is based on the technology with the slice LUTs with the schematic diagram. It contains of the flipflops, LUTs, w, x, y, z with the test mode, clock, reset with the nets, faults registers, Test pattern generator, circuit under test and output response.

Name	Slice LUTs (10400)
Built_In_Self_Test	8

Fig.7 Area of BIST

It is the coverage of the Slice LUTS with our Artix 7 FPGA Board, with the from the 10,400 we need only 8 LUTs for the BIST. The slice LUTS refer to the group of operation on the FPGA, which are interconnection to the cells in series and parallel modes.

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Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay
Path 1	∞	4	5	4	w	dataIn[0]	5.828

Fig.8 Delay of BIST

It is the time taken by the output from 0 to 50% of time, here it takes 5 sec of time for 1st path from the input to output generation. Stack refers to the any type of device verification of the infinite power of devices. Levels are Basic, Algorithmic, RTL& Switch are the 4 levels that are used in the fabrication of an IC. High fanout characteristics refer to the for the various types of inputs it has many types of characteristics, another name of High fanout is Fan in fan out characteristics. We refers to the junction wire in the FPGA with the CUT with full adder starting point..

6. Conclusion and Future Scope

Hence, We developed Built-In Self-Test (BIST) utilizing a Test Pattern Generator (TPG), a Circuit Under Test (CUT), and a Response Analyzer (RA). The TPG was constructed using a 3-bit Linear Feedback Shift Register (LFSR), while the CUT incorporated a Full Adder (FA) with the introduction of three faults to assess the functionality of the integrated circuit (IC). By Comparing of the previous author books we designed the better output graphs of output windows of BIST Simulation ,RTL Schematic of BIST, Technology schematic, Area, Power, Delay and The Response Analyzer, designed with a 4-bit LFSR, evaluates the outputs, ultimately indicating a fault-detected output. A fault-detected value of 0 signifies the absence of faults, leading to a passing system. Conversely, a fault-detected value of 1 indicates a system failure.

Now a days installation of software is easy based on coding. If the coding facility is provided to students in future studies, then student can easily install any type of software. These are all practical verification. Still it is a hope that develops the more in Hardware development in the upcoming future technology. If there is more increasing of the IC, there is increase of more demand of manufacturing. It leads to the improvement in technology 1G to 2G to 3G to 8G to 64GB technology. We know that some ICs help that working of a Sensor and work it as sensible information, more use of ICs in various still it is said to be technology development.

Hence upcoming future life gives that ICs are mostly used in fabrication with the improving methods of layers, still we need more development in testing phase. Now a days we are using the Artificial intelligence for the easy for PPTs and Chat GPT, same testing by the VHDL Codes for chip also needs the better equipment in VLSI Manufacturing methods.

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