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Improved Multicarrier PWM Technique for Harmonic Reduction by Using APOD method for Cascaded H-bridge DC/AC Converters

K Jeevan Reddy [1] , P B Charan [2], C Bhaskar Reddy [3] , M Shakthi Kumar [4] , B Vijay Kumnar [5] , V Chandu [6].

[1-6] Department of Electrical & Electronics Engineering, Mother Theresa Institute of Engineering and Technology, Palamaner-517408, Chittoor District, Andhra Pradesh.

** Corresponding Author : K Jeevan Reddy ; jeevanreddy@gmail.com*

Abstract: Conventional modulation techniques used in cascaded H-bridge multilevel (CHB) DC/AC converters often spawn the noticeable quantity of harmonics of low frequency in an output voltage. The latter usually leads to a high-peak output current, impacting adversely on performance and reliability of industrial motor drive systems. To tackle these drawbacks, this research develops an improved Multicarrier Pulse-Width Modulation (MCPWM) method based on an alternative Phase Opposition Disposition (APOD) approach. A proposed MCPWM method significantly mitigates harmonic content in an output AC voltage by keeping the continuous output current with reduced peak magnitude. A harmonic mitigation algorithm is presented, which dynamically modifies switching frequency and modulation index of semiconductor devices based on a switching angles of a MCPWM pulse. An algorithm specially deals with a 5th, 7th and 11th-order harmonics and reveals a novel range of switching angles, at which their amplitudes become minimal. One of the significant achievements of this work is the development of a novel real-time switching angle estimation technique which avoids solving complex nonlinear equations. This approach reduces not only computation time but also hardware complexity, hence making medium-capacity FPG an implementation viable. A proposed technique is authenticated by theoretical analysis, MATLAB/Simulink simulations, and exploratory verification using the three-phase FPGA-based CHB multilevel inverter prototype. Comparative analysis against state-of-the-art techniques will reveal superior efficacy of a proposed technique in terms of harmonic suppression, computational efficiency, and hardware simplicity, thus making it a practical solution for industrial power electronics applications.

Keywords: Copper nanoparticles, Carica Papaya Leaves, Biosynthesis, Biomedical.

1. Introduction

MLIs increase a quality of output voltage by generating n distinct levels of output voltage, and thus they improve a voltage waveform by the factor of (n–1) [1]. Analogize to the conventional two-level VSIs with similar power ratings, MLIs have significant merits, including a lower THD of an output voltage, lower dv/dt stress on the switching devices, and lower EMI in an output voltage [2]. These advantages enable MLIs to be applied to the wide range of applications exists, from low-voltage and low-power systems [3], medium- and high-power industrial applications [4]–[5], photovoltaic grid-connected systems [6], [7], locomotive traction [8], and a variety of specialized power-electronics applications [9]

In general, MLIs can be grouped into three main topologies:

- Neutral Point Clamped (NPC) inverters [10],
- Flying Capacitor (FC) inverters [11], [12], and
- Cascaded H-Bridge (CHB) inverters [13]–[26].

Among them, the CHB topology is of particular interest because of its intrinsic characteristics, such as modularity,

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easy scalability, and fault tolerance capability, which are of great concern in high-voltage and power applications. To further increase performance of CHB inverters, some advanced modulation techniques have been developed, including, but not limited to, an alternative Phase Opposition Disposition scheme. These techniques play a vital role in harmonic content suppression, voltage waveform quality improvement, and assuring an efficient operation of inverters, especially in industrial and high-power applications where power quality is an issue of concern.

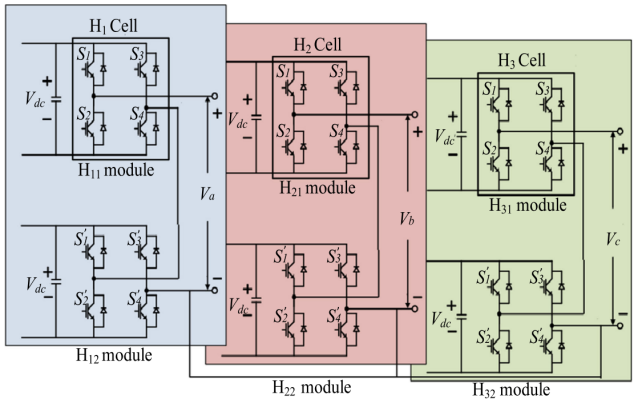

Figure. 1 Figure showing Three-Phase CHB-MLI

Among widely studied MLI topologies, Neutral Point Clamped and Flying Capacitor configurations pose certain limitations in phrase of component count and control convolution. A NPC topology requires the significant number of diodes and capacitors, and hence a more intricate control strategy has to be implemented for achieving higher output voltage levels [25]. Alternatively, although FC topology uses a comparable number of active components, it requires a larger number of capacitors and thus increases the overall system volume and complexity.

By contrast, an n-level CHB inverter consists of multiple identical low voltage H-bridge modules with separate DC power supplies, connected in cascaded configurations to synthesize the stepped output voltage waveform having n levels, as shown in Fig. 1. This topology has the following unique advantages compared to NPC and FC topologies:

Modular and scalable design allows for easy expansions through adding H-bridge modules [14].

Compatibility with soft-switching techniques, enabling use in both high- and low-voltage applications [3], [4].

Reduced electromagnetic interference (EMI) through lower dv/dt stress on semiconductor switches [2].

Flexible output level generation, where additional modules directly increase a number of output voltage levels [17].

A variety of pulse-width modulation strategies have been developed for the purpose of optimizing the performance of MLIs. These methods can generally be categorized as offline and online methods [15] or carrier-based and carrier-less techniques [16], [17].

The conventional carrier-based PWM methodology involves the comparison of a sinusoidal reference waveform with a high-frequency triangular carrier signal in order to obtain the switching signals. This method, though conventionally used because of its simplicity for industrial drive applications, creates low-frequency harmonic content, especially at high MI and higher switching frequencies [27].Among carrier-based PWM methods, an alternative Phase Opposition Disposition (APOD) technique is frequently employed in CHB inverters. In this scheme, the adjacent carrier waveforms are phase-shifted alternately by 180°, enhancing harmonic cancellation and lowering THD in an output voltage. Compared to the other strategies such as Phase Disposition (PD) and Phase Opposition Disposition (POD), APOD can achieve superior harmonic performance while maintaining a relatively simple implementation, making it very suitable for modular and scalable CHB configurations.

The SVPWM is a more advanced modulation technique for MLIs. It allows for direct control of the phase voltages and line-to-line voltages and provides the possibility to use the redundancy in the switching states and the voltage vectors to minimize common-mode voltages. It is increasingly applied in power electronics due to its capacity to enhance voltage utilization and harmonic performance.

The generalized 2D and 3D SVPWM algorithms for n-level inverters are shown in [18]. These generally involves a process of nearest voltage vectors selection, dwell times calculation and sequencing of switching transitions. However, the SVPWM real-time implementation is computationally challenging due to its extensive computational resource requirement and determination of switching angles.

The MCPWM technique has so far remained the conventional approach for controlling an AC output of CHB inverters [22]. It relies on n−1 triangular carrier signals dispersed in voltage bands between and, where Vdc is a DC input voltage. An APOD setup, when adopted for implementation of MCPWM, improves harmonic dispersion while successfully cancelling some of the low-order harmonics.

These harmonics might include a fifth, seventh, and eleventh orders that conventional MCPWM methods are not capable of completely eliminating [25]–[29]. In turn, several harmonic mitigation approaches have recently been presented. The mathematical formulation for

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suppressing nontriplen harmonics was first presented in [25], while in [27], one FPGA-based HDSPWM method was developed for yielding high-resolution PWM signals with minimum EMI. This approach minimizes power losses while maintaining a high quality output, therefore having the potential to further improve the conventional MCPWM schemes.

During recent years, many methods have been proposed to reduce harmonic content in the inverter output waveforms [16], [19]–[25]. In medium-voltage and high-power drive applications, both the switching losses and EMI need to be reduced. Soft-switching PWM methods that have recently gained widespread acceptance for this purpose include SHE and SHM methods [25]. A nonlinear equation is solved in these methods in order to obtain the optimal switching angles that eliminate or mitigate particular harmonic orders.

In [20] and [24], various SHE-PWM models were analyzed, including a new method for reducing the circulating currents in modular MLIs based on (n+1) SHE-PWM, by setting a modulation index across inverter arms. While effective, such methods are plagued by the computational burden of solution of nonlinear equations in real time. Other approaches, such as an use of Groebner bases and symmetric polynomials for switching angle determination [23], also face similar obstacles in implementation complexity.

In this paper control technique with improved MCPWM is presented for the five-level CHB VSI. A proposed method focuses on:

- Smoothing a 5th, 7th, and 11th-order harmonics from a phase output voltage,
- Ensuring ripple-free output current,
- Improving general power quality of an inverter.

Instead of dealing with complicated nonlinear sets of equations, one method uses the set of low-order equations to estimate fundamental voltage amplitude for variable switching angles. This enables the identification of the domain of switching angle that minimizes the targeted harmonics without incurring high computational costs.

The algorithm has been implemented in an APOD-based multicarrier PWM framework to achieve robust harmonic performance for diversified operating conditions. The simulated results are also in close agreement with the theoretical predictions, hence confirming the effectiveness of the proposed approach for industrial and high-performance applications.

2. Mathematical Analysis of APOD SPWM

In this section, the mathematical analysis of an alternative Phase Opposition Disposition (APOD) Sinusoidal Pulse Width Modulation (SPWM) technique will be developed. This includes the derivation of equations of a carrier signal, modulating signal, a switching condition, a phase shift in an APOD method, and an output waveform generated by a modulation technique.

Carrier Signal Representation

The triangular or sawtooth waveform is generally the carrier signal in SPWM techniques. In an APOD SPWM method, these carriers are modulated with specific phase shifts to produce a smoother output waveform with reduced harmonic content.

Triangular Carrier Signal:

For a k-th carrier, the triangular carrier signal, Ck(t), in an APOD technique can be represented as:

$$C_k(t) = A_c \cdot \text{sign}\left(\sin\left(2\pi f_c t + \phi_k\right)\right)$$

Where:

- Ac is an amplitude of a carrier,
- fc is a frequency of a carrier, which is commonly much higher than the frequency of a modulating signal,
- ϕk is a phase shift applied to a k-th carrier,
- t is time.

The **sign** function outputs the waveform that alternates between +Ac and −Ac, creating a triangular shape.

Carrier Phase Shift:

The carriers in APOD are phase-shifted to create phase opposition. A phase shifts alternate between consecutive carriers to produce the symmetric waveform. For a k-th carrier, a phase shift is given by:

$$\phi_k = \pm\frac{k\pi}{N}$$

Where:

- N is a total number of carriers (which depends on a number of levels in an inverter),
- k is an index of a carrier signal, which ranges from 1 to N.

Thus, for the 5-level inverter with 5 carriers, a phase shifts would be alternated as:

$$\phi_1 = 0^\circ,$$
$$\phi_2 = +\frac{\pi}{5},$$
$$\phi_3 = -\frac{\pi}{5},$$
$$\phi_4 = +\frac{2\pi}{5},$$
$$\phi_5 = -\frac{2\pi}{5}.$$

This results in the set of carriers with alternating phase shifts that are oppositely phased with respect to one another.

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Reference Signal Representation

The **reference signal**, also known as a **modulating signal**, is typically the **sinusoidal waveform** that determines a desired output voltage. A modulating signal is contrast with a carrier signals to generate a PWM signal. A modulating signal M(t) can be expressed as:

$$M(t) = A_m \cdot \sin(2\pi f_m t)$$

Where:

- A_m is an amplitude of a modulating signal (typically determined by a desired output voltage),
- f_m is a frequency of a modulating signal (which is a desired output frequency of an inverter),
- t is time.

The amplitude and frequency of a modulating signal control a characteristics of an output waveform, with a modulating signal essentially shaping an envelope of an output.

Switching Condition for APOD SPWM

The switching condition for an APOD SPWM technique determines a moments when an inverter switches between different voltage levels. In a standard SPWM technique, a switching points occur when a modulating signal intersects a carrier signal. Similarly, in APOD SPWM, a switching points are determined by an intersections between a phase-shifted carriers and a modulating signal.

Condition for Switching:

A switching event occurs whenever a modulating signal M(t) intersects a carrier signal Ck(t). Mathematically, this is represented as:

$$M(t) = C_k(t)$$

Substituting an expressions for M(t) and Ck(t):

$$A_m \cdot \sin(2\pi f_m t) = A_c \cdot \text{sign}\left(\sin\left(2\pi f_c t + \phi_k\right)\right)$$

This equation represents a condition for an inverter to switch from one voltage level to another.

Analysis of Intersections:

- The intersections occur when a modulating sine wave intersects a triangular carrier wave at specific instants in time. A phase shift ϕk changes a location of these intersections for each carrier signal.
- For example, if a modulating signal intersects a carrier at the specific time t1, an inverter will switch to the particular voltage level corresponding to a carrier signal's state at that time.

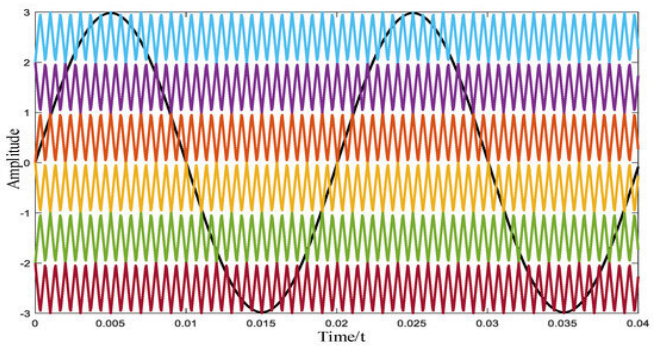

Figure 2. Carrier and modulation of APOD MC PWM waveform with 1 kHz frequency

Carrier Phase Shift in APOD

The **carrier phase shift** is a key feature of an APOD method that distinguishes it from other modulation techniques. By alternating a phase shifts of a carriers, an APOD method aims to **spread a harmonic content** over the broader range of frequencies, thereby reducing low-order harmonic distortion.

Derivation of a Phase Shift:

The phase shift for a k-th carrier in an APOD method can be expressed as:

$$\phi_k = \pm\frac{k\pi}{N}$$

Where k is an index of a carrier, ranging from 1 to N, and N is a number of carriers used for modulation (which is typically equal to a number of levels in an inverter).

For eg, for the 5-level inverter (N=5):

Carrier 1 has a phase shift of $\phi_1 = 0°$,

Carrier 2 has a phase shift of $\phi_2 = +\frac{\pi}{5}$,

Carrier 3 has a phase shift of $\phi_3 = -\frac{\pi}{5}$,

Carrier 4 has a phase shift of $\phi_4 = +\frac{2\pi}{5}$,

Carrier 5 has a phase shift of $\phi_5 = -\frac{2\pi}{5}$.

This alternating phase shift ensures that a **carrier signals are oppositely phased**, thus reducing harmonic content by spreading a switching events across the wider frequency range. A result is the smoother, more sinusoidal output waveform with lower total harmonic distortion (THD).

V. Proposed CHB Multilevel Inverters

Proposed three-phase seven-level inverter topology

The proposed seven-level three-phase inverter architecture is composed of two key sections. A **first section** is the three-phase full-bridge inverter, referred as a **main circuit**. A **second section**, known as an a**uxiliary circuit**, includes **two asymmetrical half-bridge sub circuits per phase**, as illustrated in **Fig. 1**.

The auxiliary circuit utilizes DC voltage sources of **E** and **2E**, while a main inverter operates with the DC input of **–3E**. A role of a main circuit is to produce a negative voltage levels, enabling an inverter to output **bipolar phase voltages** without requiring the polarity-inverting bridge in an auxiliary circuit. As the result, each auxiliary cell is composed of only **two switching devices**, enhancing a design's simplicity and efficiency.

The inverter system requires the total of **18 IGBTs** and **7 separate DC sources**. By accurately managing a switching states in each phase, an output voltages V_a, V_b, and V_c can

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be synthesized accordingly. These output phase voltages are derived as follows:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{a1} & S_{a2} & S_{a3} \\ S_{b1} & S_{b2} & S_{b3} \\ S_{c1} & S_{c2} & S_{c3} \end{bmatrix} \times \begin{bmatrix} 1 \\ 2 \\ -3 \end{bmatrix} E$$

where Sx1,Sx2, and Sx3 are a switching states of a main circuit and two auxiliary stages for phase ∀x=a,b,c, respectively, such that;

$$S_{xi} = \begin{cases} 1 & if\ the\ switch\ S_{xi}\ is\ on \\ 0 & if\ the\ switch\ S_{xi}\ is\ of \end{cases} \quad (\forall\ i = 1, 2, 3)$$

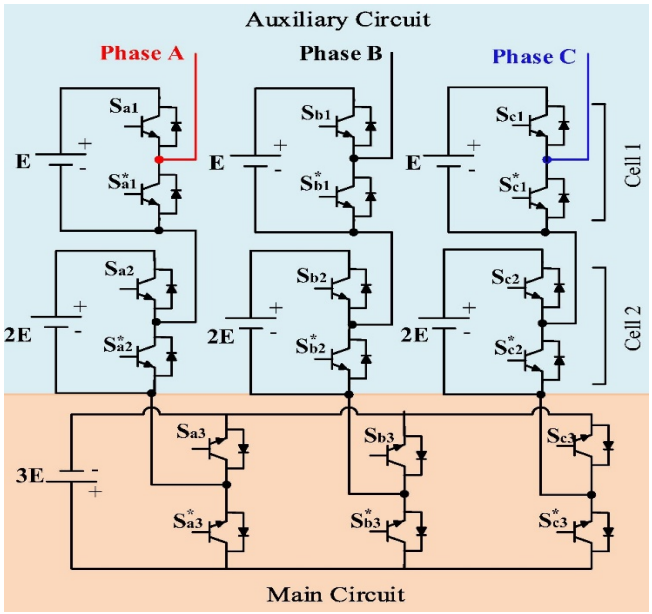

Figure. 2 Schematic figure of a proposed multilevel inverter configuration

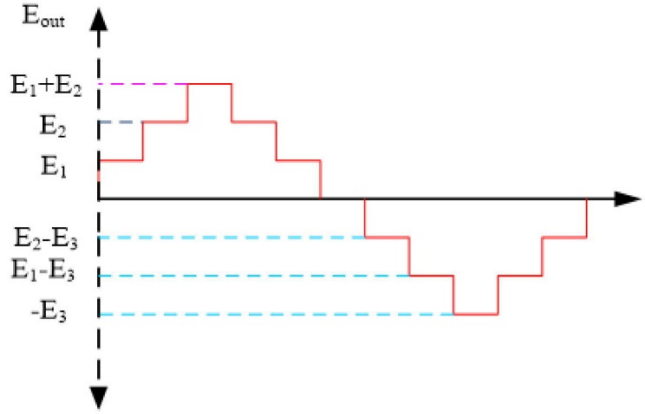

Figure. 3 Output voltage levels

The proposed configuration is simpler, cost-effective, and better suited for efficient switching strategies. A switching sequence required to produce a three-phase output voltages for a 7-level inverter is discussed in a next section. As shown in Fig. 1, a structure of a proposed inverter consists of individual cells, each formed by connecting the DC bus voltage across two IGBT switches operating in the complementary manner. An applied DC voltage is used to increase a number of output voltage levels. Furthermore, a number of output phases can be expanded, as illustrated in Fig. 3.

Table 2 presents switching patterns for phases A, B, and C, utilizing six switches and three independent DC sources per phase. This arrangement effectively generates the seven-level output voltage waveform.

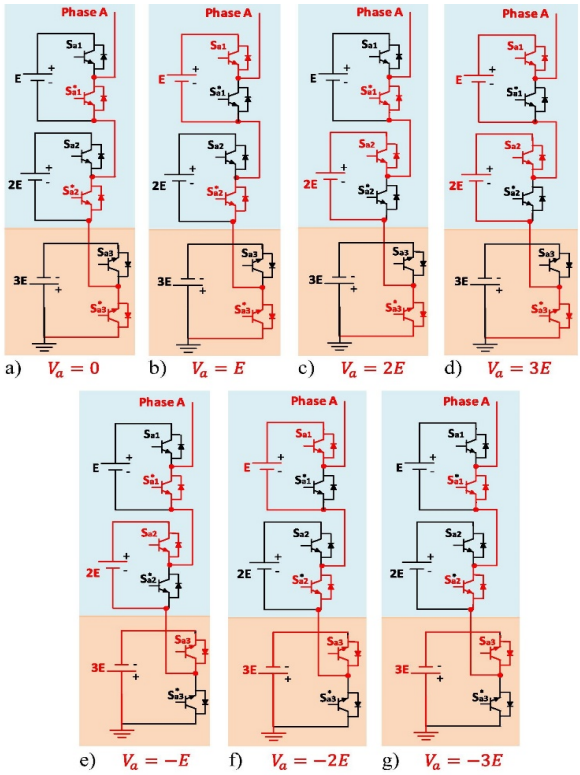

Figure. 4 Switching sequence for Phase the of a proposed 7-level inverter

Principle of Operation of a Proposed MLI

This section details a generation process for a three-phase 7-level output voltage waveform, as illustrated in **Fig. 2**. To achieve the symmetrical three-phase output, a switching sequences for each phase are identical but shifted by 120° (2π/3 radians). Therefore, an operation of an inverter is demonstrated using only Phase A, as other phases follow a same sequence with appropriate phase shifts.

Figure.3 illustrates a seven distinct switching states responsible for producing a corresponding output levels in Phase A. A red paths in a diagram indicate a current conduction routes for each switching state. As shown, a positive voltage levels are produced using an auxiliary cells, while a negative voltage levels are derived either entirely from a main circuit or through the combination of both a main and auxiliary circuits.

A detailed list of a switching states that generate a seven voltage levels for Phase the is provided in

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Table. 1 Switching table for phase A

	auxiliary cell 1		auxiliary cell 2		main circuit		
state	S_{a1}	S^*_{a1}	S_{a2}	S^*_{a2}	S_{a3}	S^*_{a3}	V_a
1	0	1	0	1	0	1	0
	1	0	1	0	1	0	
2	1	0	0	1	0	1	+E
3	0	1	1	0	0	1	+2E
4	1	0	1	0	0	1	+3E
5	0	1	1	0	1	0	−E
6	1	0	0	1	1	0	−2E
7	0	1	0	1	1	0	−3E

Modular Operation of a Proposed MLI

The proposed three-phase MLI has the modular design that allows scalability and flexibility. The modularity permits a system to be extended by connecting the conventional three-phase full-bridge inverter in series with j unsymmetrical half-bridge auxiliary cells per phase. Each auxiliary cell operates with its own independent DC source, supplied at distinct voltage levels.

The DC voltage level for every auxiliary cell i can be defined by the following relationship:

$$V_{dc(i)} = 2^{i-1}E \qquad \forall(i = 1, 2, \dots j)$$

Here, **E** denotes a voltage corresponding to the single level. A DC voltage of a main three-phase full-bridge inverter, denoted as $\mathbf{V_{dcm}}$, must be equal to a negative sum of a DC voltage levels of all an auxiliary cells. This ensures proper voltage balancing and facilitates a generation of symmetric bipolar output waveforms.

$$V_{dc(m)} = \sum_{i=1}^{j} -\left(2^{i-1}E\right)$$

The main circuit DC voltage level is negative due to its principal responsibility of providing negative output voltage levels. In this topology, the maximum phase output voltage is determined by the sum of the DC voltage levels fed to the auxiliary cells. Thus, n, as the maximum number of output phase voltage levels, can be derived from the total number of auxiliary cells by the following relation:

$$n = \frac{\sum_{i=1}^{j}\left(2^{i-1}E\right)}{E} = \sum_{i=1}^{j} 2^{i-1}$$

As the result, a highest number of output **line voltage** levels, denoted by mmm, can be determined using a following expression;

$$m = 2n + 1 = 1 + \sum_{i=1}^{j} 2^i = 2^{j+1} - 1$$

Therefore, in order to increase the number of voltage levels in an output, the number of auxiliary cells has to be increased correspondingly. However, adding one more auxiliary cell will result in adding six power switches and three isolated DC sources in each phase, as can be seen from Fig. 3. Thus, the overall number of power switches (N_s N_s N_s) and isolated DC sources (N_p s N_{p s} N_p s) can be presented by the number of auxiliary cells as:;

$$N_s = 6(j + 1)$$

By substituting Equation (6) into Equations (7) and (8), an expressions for a number of power switches and isolated DC supplies can be reformulated as functions of a number of line voltage levels per pole, as shown below;

$$N_s = \frac{6\ln(m+1)}{\ln 2}$$

$$N_{Ps} = \frac{3\ln(m+1)}{\ln 2} - 2$$

These relationships are valuable for evaluating a proposed three-phase MLI against other multilevel inverter topologies. Additionally, a proposed inverter design can be scaled into the multi-phase MLI by incorporating additional legs into an existing three-phase configuration.

3. Mathematical Derivation of THD in APOD SPWM

3.1 Harmonic Analysis in APOD SPWM

To evaluate a harmonic distortion in an alternative Phase Opposition Disposition (APOD) sinusoidal PWM technique, an individual harmonic components must first be identified. Once these components are known, a Total Harmonic Distortion (THD) can be computed to assess waveform quality.

Influence of Carrier Arrangement on THD

In APOD SPWM, an arrangement of carrier signals—specifically their number and phase displacement—has the significant effect on THD. Increasing the number of carriers makes a waveform more similar to a pure sinusoidal signal, hence decreasing harmonic distortion. The lower the number of carriers or voltage levels, the coarser an approximation of a sinusoidal waveform will be, which tends to raise THD.

3.1. Switching Frequency Optimization Concept

- Optimization of the switching frequency means adjustment of an inverter's switching frequency with the view of having a desirable harmonic profile. A switching frequency defines the speed at which an inverter toggles between voltage levels. The harmonic performance will improve by optimizing f_s, resulting in a cleaner output signal.
- Generally speaking, higher switching frequencies reduce harmonic distortion because they allow for finer modulation of an output voltage, making it more closely resemble the sine wave. However, this improvement comes at a cost: higher switching losses and reduced system efficiency. An optimum balance has to be maintained, therefore.
- Mathematical Model for Switching Frequency Optimization

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Switching frequency f_s can be dynamically adjusted based on certain system requirements such as load conditions or target waveform fidelity. An optimization goal can be in the minimization of THD by fine-tuning a switching frequency. This can be mathematically represented by a following objective function:

$$\min_{f_s} \text{THD}(f_s)$$

Where:

- **THD(f_s)** denotes a Total Harmonic Distortion as the function of switching frequency.
- **f_s** is a variable switching frequency.

This optimization framework seeks a frequency value that offers a lowest possible THD while also managing a trade-off with switching losses. A result is the more efficient and higher-quality inverter output suitable for practical applications.

4. Adaptive Modulation and Phase Shifting

4.1. Adaptive Modulation Index

SPWM modulation index mmm is defined as the ratio between the peak amplitude of the modulating signal Am and the peak amplitude of the carrier signal Ac:

$$m = \frac{A_m}{A_c}$$

The width of the pulses generated by the PWM technique will be determined by the modulation index; a high value of the latter increases the width of the pulses, and vice versa. In systems with adaptive modulation, a modulation index can be dynamically adjusted based on load variations or real-time feedback of harmonic distortion. When a load varies, a modulation index is adjusted to optimize an output waveform and reduce harmonic distortion.

Table. 2 Comparison Analysi

Feature	Carrier-Based PWM	SVM	APOD SPWM
Simplicity	Simple to implement	Complex, requires vector calculation	Moderate complexity, requires phase shifting
Harmonic Mitigation	Moderate, harmonics concentrated at low frequencies	Excellent, reduces harmonics significantly	Good, reduces low-order harmonics effectively
Voltage Quality	Poor in high levels, better in lower levels	Excellent, higher voltage utilization	Very good, smoother output with reduced THD
Efficiency	Moderate, losses due to harmonic content	High, due to better voltage utilization	High, improved by reduced harmonic distortion
Application	Low- to medium-power inverters	High-power, high-efficiency inverters	Suitable for medium- to high-power systems

4.2. Phase Shifting for Harmonic Mitigation

In addition to modulation index adjustment, adaptive phase shifting can be employed to further reduce harmonic distortion. Phase shifting refers to a process of adjusting a relative phase of a carrier signals to minimize harmonic content. During APOD SPWM, the carrier signals are phase-shifted to create opposite phases in order to reduce low-order harmonics.

Mathematically, a phase shift ϕk for a k-th carrier can be adjusted as the function of a load:

$$\phi_k(t) = \pm\frac{k\pi}{N} + \Delta\phi(t)$$

Where:

$\Delta\phi$(t) is a dynamic phase shift adjustment based on load conditions,
\tN is a number of carriers,
\tk is an index of a carrier.

This dynamic phase shifting ensures that a harmonic content remains minimal across varying loads, improving overall inverter performance.

5. Mathematical Representation of APOD SPWM

In an APOD SPWM technique, a **carrier signals** are triangular waves, and they are phase-shifted in such the way that a phase displacement between adjacent carriers is 180°. Mathematically, a carrier signals for the **5-level inverter** can be expressed as:

$$C_i(t) = A \cdot \text{triangle}\left(f_c t + \Phi_i\right), \quad \Phi_i = 180^\circ \times (i-1) \quad \text{for} \quad i = 1, 2, 3, \ldots, N$$

where:

Ci(t) is an i-th carrier signal,
an is an amplitude of a carrier signal,
fc is a carrier frequency,
Φi is a phase shift applied to each carrier signal,
N is a number of carriers.

The **modulating sine wave** is compared against these carrier signals, and a switching points are determined when a modulating signal intersects a carrier wave. This modulation technique results in **reduced harmonic distortion** and smoother

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voltage waveforms, which help mitigate issues like torque ripple and high-peak output current. **APOD SPWM vs. Carrier-Based PWM vs. SVM:**

6. Results

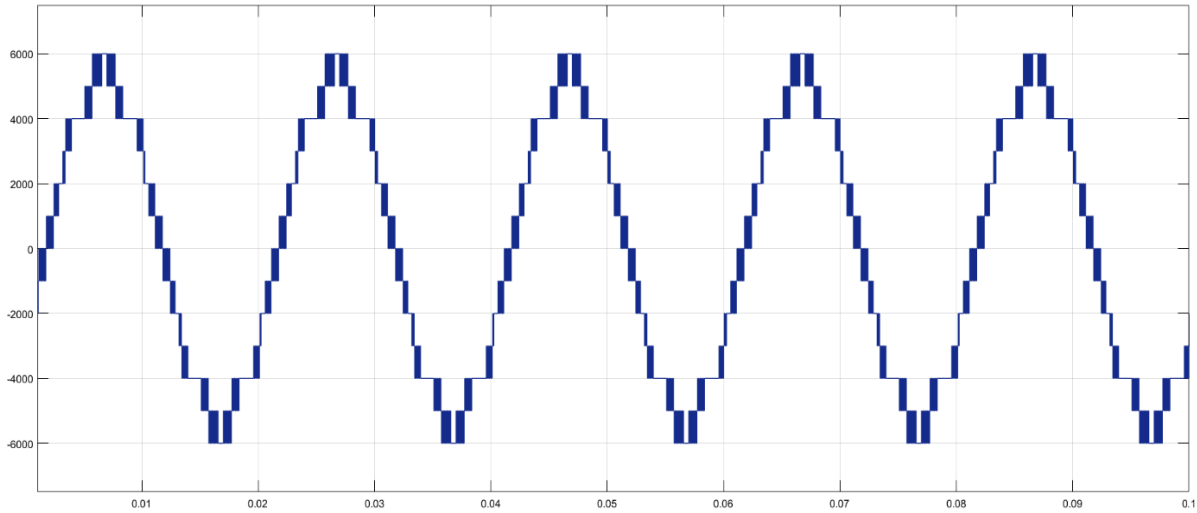

Figure. 5 13 level output voltage of a proposed converter

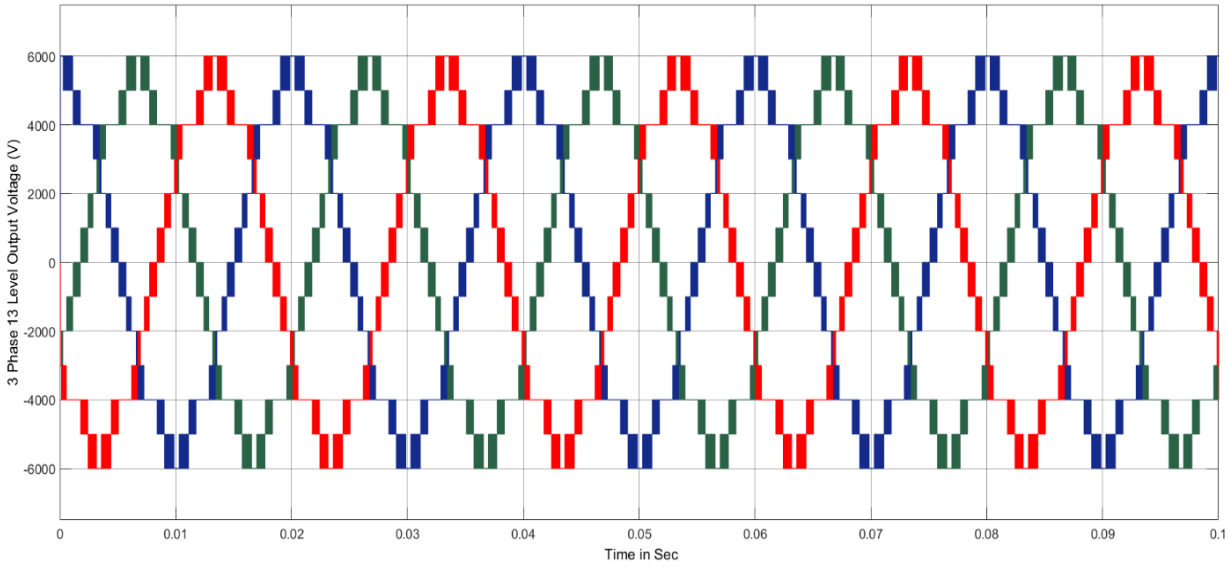

Figure. 6 3 phase 13 level output voltage of a proposed converter with APOD SPWM

Fourier Series for APOD SPWM Output:

The output voltage Vout(t) of an APOD-modulated inverter is the sum of sinusoidal components with different frequencies. As mentioned, we can represent it as:

$$V_{\text{out}}(t) = V_1 \cdot \sin(2\pi f_m t) + \sum_{n=2}^{\infty} V_n \cdot \sin(2\pi n f_m t + \theta_n)$$

Where:

- V1 is an amplitude to fundamental frequency,
- Vn is an amplitude to n-th harmonic,
- fm is a frequency to modulating signal,
- θn is a phase shift to n-th harmonic.

4.3 Calculation to THD:

Once an amplitudes to a harmonic components are known, we can calculate a **Total Harmonic Distortion (THD)** as:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{N} V_n^2}}{V_1}$$

Where:

- V1 is an amplitude to a fundamental component,
- Vn is an amplitude to a n-th harmonic component,
- N is a highest harmonic to consider (usually limited to the finite number to harmonics based on system specifications).

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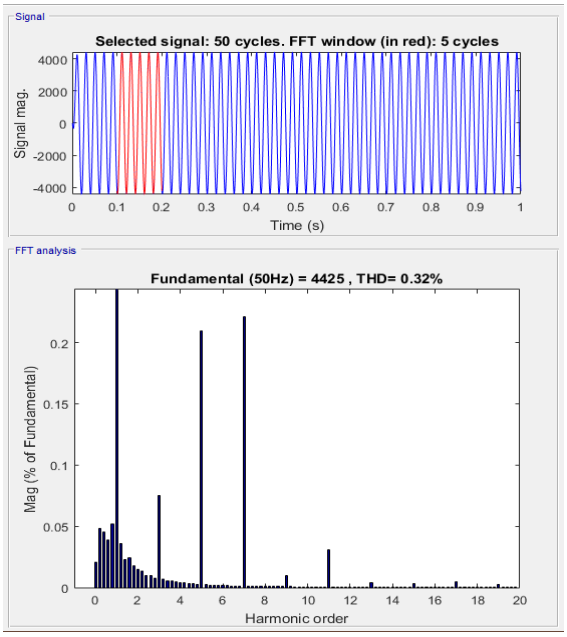

Figure. 7 THD % to a 3 phase 13 level output voltage to a proposed converter with APOD SPWM

7. Conclusion

Cascaded H-Bridge (CHB) inverters, due to their multi-level topology, offer significant advantages in high-power and high-voltage applications by reducing voltage stress on switching components and improving system efficiency. However, they can introduce challenges such as low-frequency harmonic distortion and discontinuous high-peak current, which can negatively impact a performance to industrial motor drive systems. These issues can result in torque ripple, reduced motor efficiency, and increased wear and tear on a motor, ultimately affecting system reliability and operational costs. The integration to Alternative Phase Opposition Disposition (APOD) Sinusoidal Pulse Width Modulation (SPWM) serves as an effective solution to these challenges. By applying phase opposition between a carrier signals, APOD SPWM helps to distribute a harmonic content across higher frequencies and reduce an amplitude to low-frequency harmonics, which are primarily responsible for torque ripple and current discontinuities.

This modulation technique significantly improves an output voltage waveform, leading to the smoother current profile, reduced torque ripple, and enhanced motor performance. Moreover, the application to APOD SPWM in Cascaded H-Bridge inverter reduces harmonic distortion and at the same time optimizes overall system efficiency, hence becoming the highly beneficial approach in motor drive systems. In this way, one will ensure not only more stable operation and longer motor life but also higher energy efficiency, increasing overall reliability for industrial applications.

In conclusion, whereas the basic CHB inverters present several challenges in motor drive systems, the adoption of advanced modulation techniques like APOD SPWM can considerably raise their performance and offer a robust solution for harmonic mitigation and improved power quality. Industry demands for high-performance motor drives and energy-efficient solutions continue to increase, and thus a combination of CHB inverters and APOD SPWM will most probably be an increasingly popular choice to achieve optimal motor control with efficient system operation.

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